

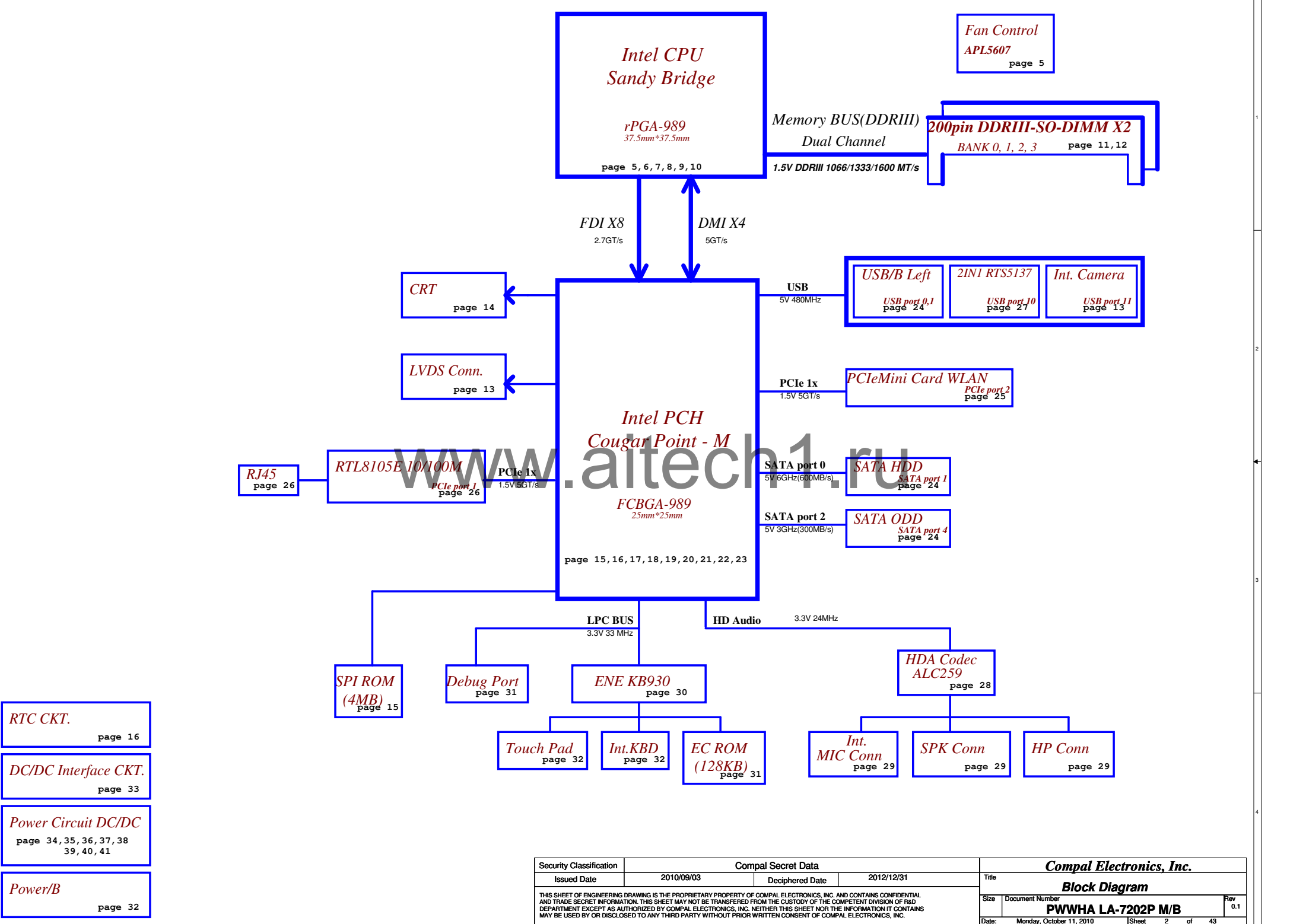
PWWHA

Delhi 10R

LA-7202P REV 0.1 Schematic

Intel Processor (Sandy Bridge) / PCH (Cougar Point)
2010-10-12 Rev 0.1

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RTC CKT.

page 16

DC/DC Interface CKT.

page 33

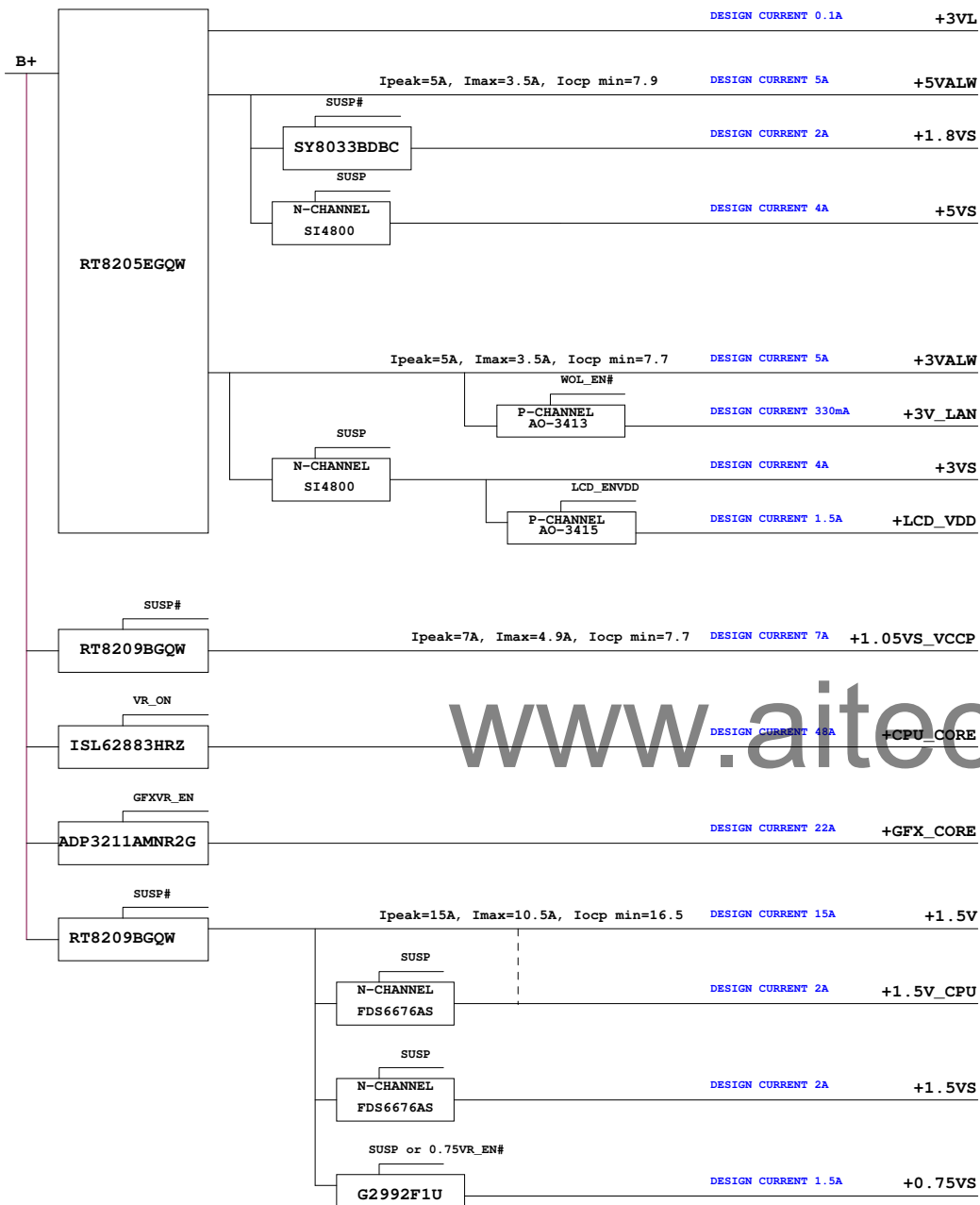
Power Circuit DC/DC

page 34, 35, 36, 37, 38, 39, 40, 41

Power/B

page 32

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Voltage Rails (O MEANS ON X MEANS OFF)

power plane \ State	+RTCVCC	B+	+3VL	+5VALW +3VALW +VSB	+1.5V	+5VS +3VS +1.8VS +1.5VS +1.05VS +0.75VS +CPU_CORE +GFX_CORE
S0	O	O	O	O	O	O
S1	O	O	O	O	O	O
S3	O	O	O	O	O	X
S5 S4/AC	O	O	O	O	X	X
S5 S4/ Battery only	O	O	O	X	X	X
S5 S4/AC & Battery don't exist	O	X	X	X	X	X

PCH SM Bus Address

Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b
+3VS	Clock Generator	D2 H	1101 0010 b
+3VS	WLAN/WIMAX		

EC SM Bus1 Address

Power	Device	HEX	Address
+3VL	Smart Battery	16 H	0001 0110 b

EC SM Bus2 Address

Power	Device	HEX	Address
+3VS	PCH	96 H	1001 0110 b

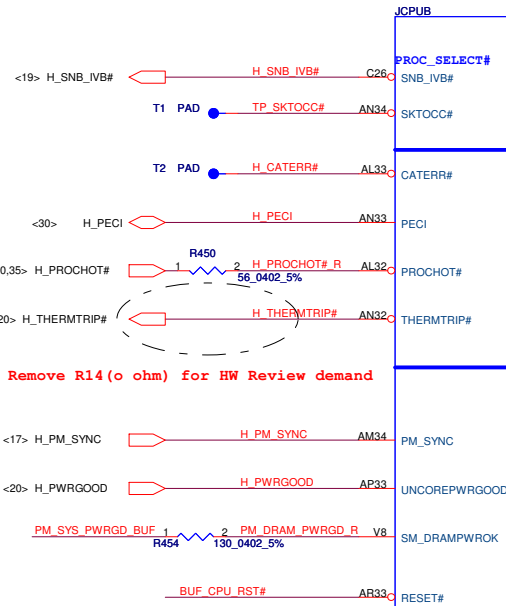
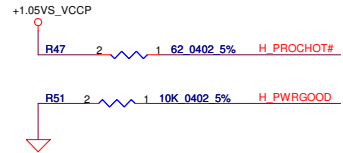
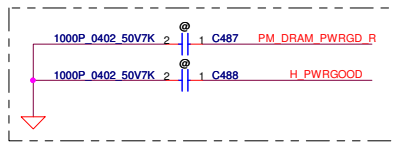
BTO Option Table

Function	MINI PCI-E SLOT		LAN				
description			SLOT1	LAN			
explain			WLAN/BT	10/100M			
BTO							

Function				Camera & Mic		
description				Camera & Mic		
explain				Camera & Mic		
BTO				CAM@		

Function	S3 Power Saving	
description	S3 Power Saving	
explain	Power Saving	
BTO		

STATE \ SIGNAL	SLP_S3#	SLP_S4#	SLP_S5#
Full ON	HIGH	HIGH	HIGH
S1 (Power On Suspend)	HIGH	HIGH	HIGH
S3 (Suspend to RAM)	LOW	HIGH	HIGH
S4 (Suspend to Disk)	LOW	LOW	HIGH
S5 (Soft OFF)	LOW	LOW	LOW
G3	LOW	LOW	LOW



Remove R14 (0 ohm) for HW Review demand

JCPU
PROC_SELECT#
SNB_IVB#
SKTOCC#
CATERR#
PECI
PROCHOT#
THERMTRIP#
PM_SYNC
UNCOREPWRGOOD
SM_DRAMPWROK
RESET#

THERMAL

PWR MANAGEMENT

MISC

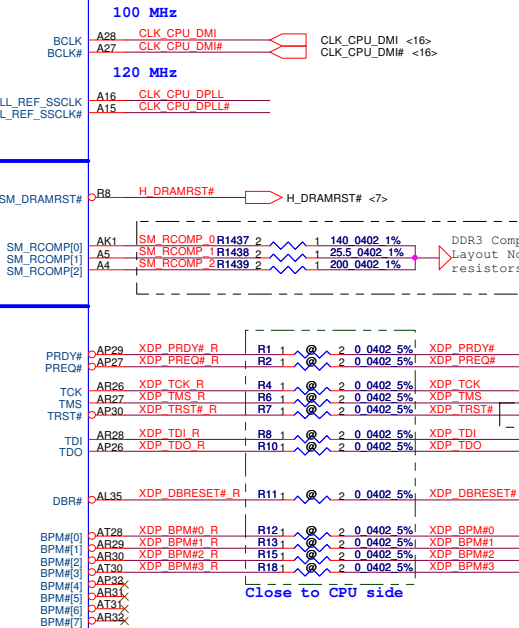
DDR3

JTAG & BPM

CLOCKS

MISC

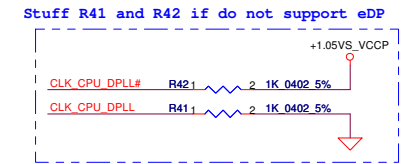
JTAG & BPM



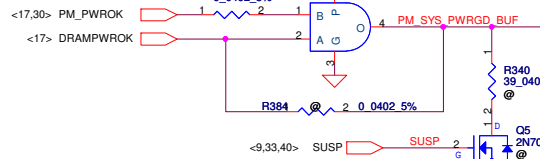
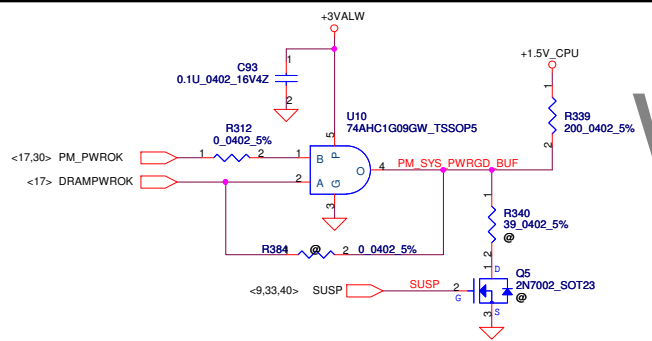
100 MHz

120 MHz

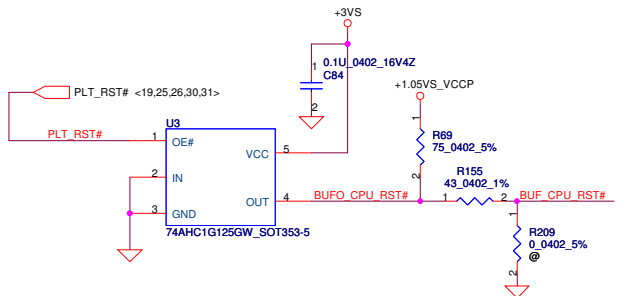
Close to CPU side



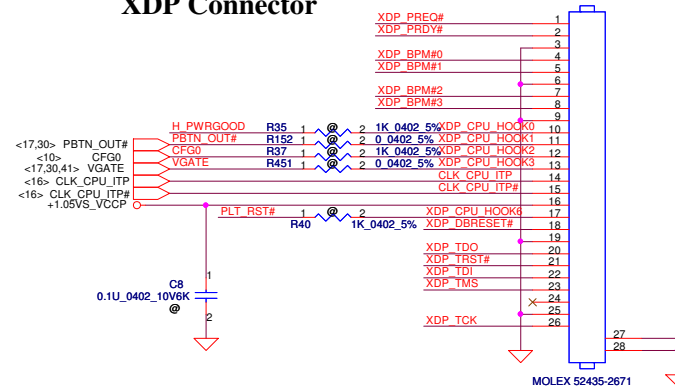
Stuff R41 and R42 if do not support eDP



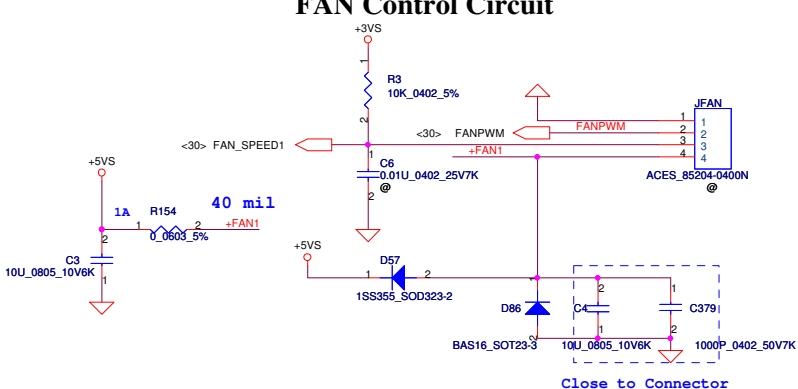
Buffered Reset to CPU



XDP Connector



FAN Control Circuit



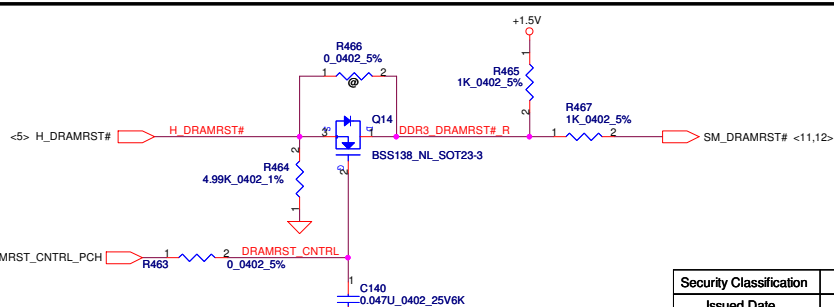
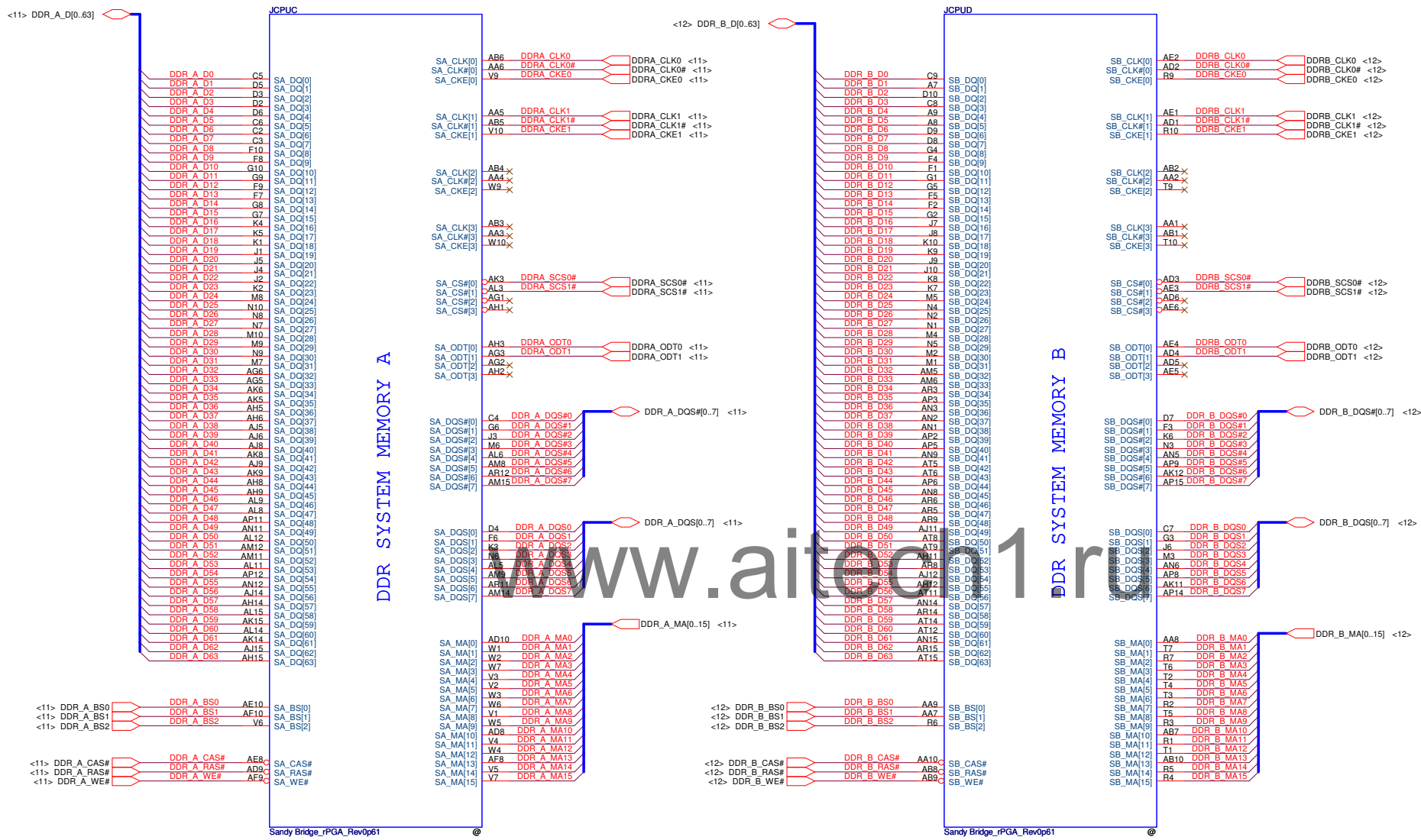
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PEG_ICOMPI and RCOMPO signals should be shorted and routed with - max length = 500 mils - typical impedance = 43 m ohm (4 mils)

PEG_ICOMPO signals should be routed with - max length = 500 mils - typical impedance = 14.5 m ohm (12 mils)

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POWER

53A (SV 35W)

8.5A

PEG AND DDR

CORE SUPPLY

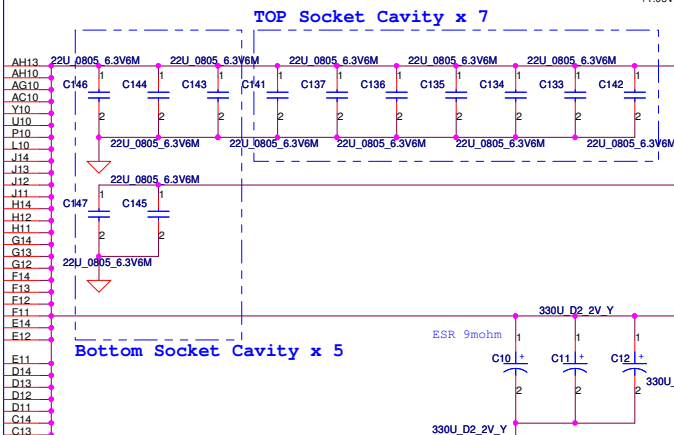
SVID

SENSE LINES

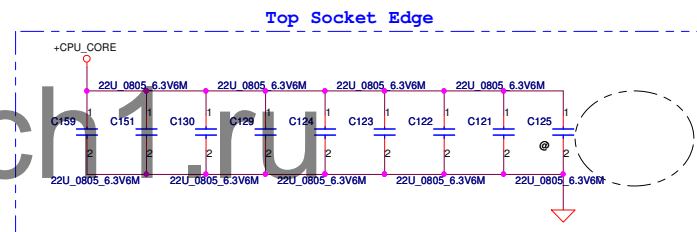
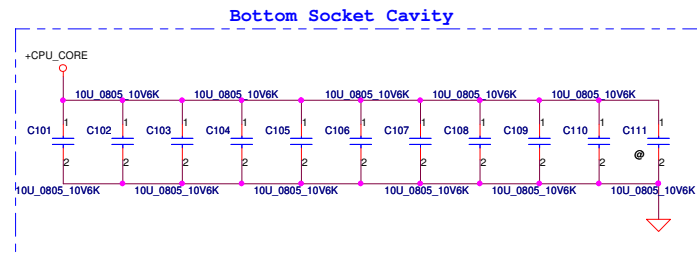
- AG35 VCC1
- AG34 VCC2
- AG33 VCC3
- AG32 VCC4
- AG31 VCC5
- AG30 VCC6
- AG29 VCC7
- AG28 VCC8
- AG27 VCC9
- AG26 VCC10
- AF35 VCC11
- AF34 VCC12
- AF33 VCC13
- AF32 VCC14
- AF31 VCC15
- AF30 VCC16
- AF29 VCC17
- AF28 VCC18
- AF27 VCC19
- AD35 VCC20
- AD34 VCC21
- AD33 VCC22
- AD32 VCC23
- AD31 VCC24
- AD30 VCC25
- AD29 VCC26
- AD28 VCC27
- AD27 VCC28
- AD26 VCC29
- AC35 VCC30
- AC34 VCC31
- AC33 VCC32
- AC32 VCC33
- AC31 VCC34
- AC30 VCC35
- AC29 VCC36
- AC28 VCC37
- AC27 VCC38
- AC26 VCC39
- AA35 VCC40
- AA34 VCC41
- AA33 VCC42
- AA32 VCC43
- AA31 VCC44
- AA30 VCC45
- AA29 VCC46
- AA28 VCC47
- AA27 VCC48
- AA26 VCC49
- Y35 VCC50
- Y34 VCC51
- Y33 VCC52
- Y32 VCC53
- Y31 VCC54
- Y30 VCC55
- Y29 VCC56
- Y28 VCC57
- Y27 VCC58
- Y26 VCC59
- Y25 VCC60
- V34 VCC61
- V33 VCC62
- V32 VCC63
- V31 VCC64
- V30 VCC65
- V29 VCC66
- V28 VCC67
- V27 VCC68
- V26 VCC69
- U35 VCC70
- U34 VCC71
- U33 VCC72
- U32 VCC73
- U31 VCC74
- U30 VCC75
- U29 VCC76
- U28 VCC77
- U27 VCC78
- U26 VCC79
- R35 VCC80
- R34 VCC81
- R33 VCC82
- R32 VCC83
- R31 VCC84
- R30 VCC85
- R29 VCC86
- R28 VCC87
- R27 VCC88
- R26 VCC89
- R25 VCC90
- P35 VCC91
- P34 VCC92
- P33 VCC93
- P32 VCC94
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- P29 VCC97
- P28 VCC98
- P27 VCC99
- P26 VCC100

Sandy Bridge_rPGA_Rev0p61

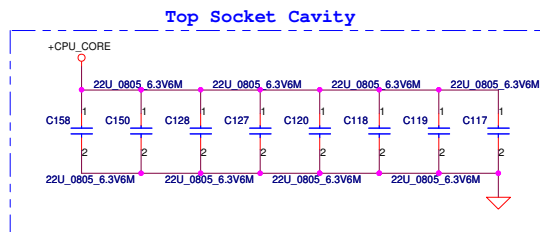
+1.05VS_VCCP Decoupling:
2X 330U (6m ohm), 12X 22U



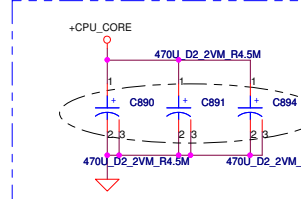
+CPU_CORE Decoupling:
4X 470U (4m ohm), 16X 22U, 10X 10U



9/02 Remove C126, C131 by Power Demand



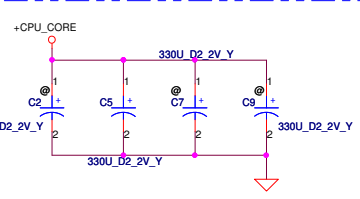
Co-Lay with C2, C5, C7, C9



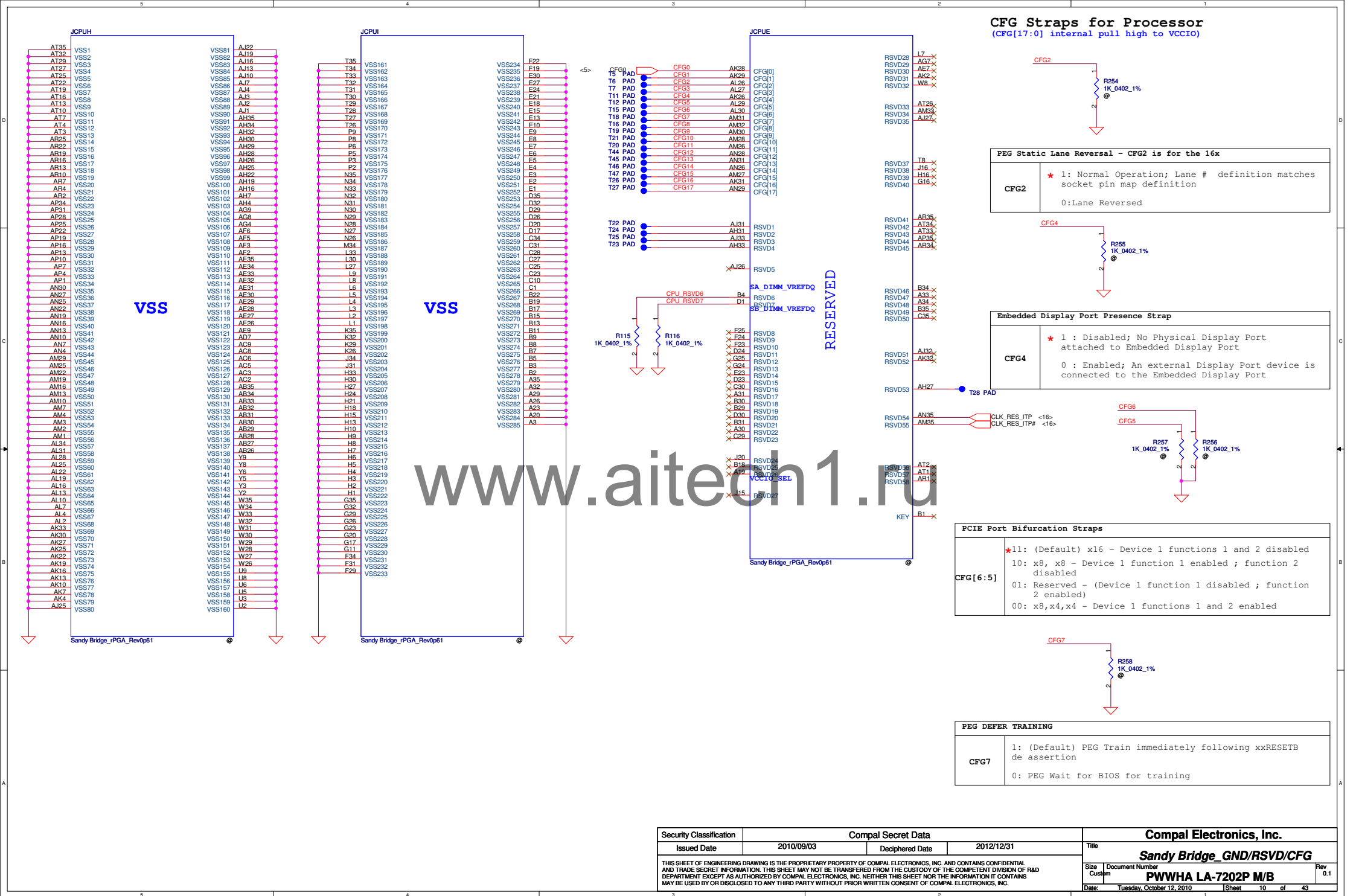
9/02 Add C898 3Pin Bulk Cap by Power Demand

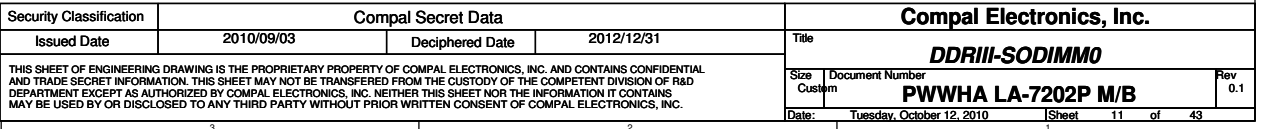
9/02 Change C890, C891, C894 from SGA00005R00 to SGA00004X80 for Power demand

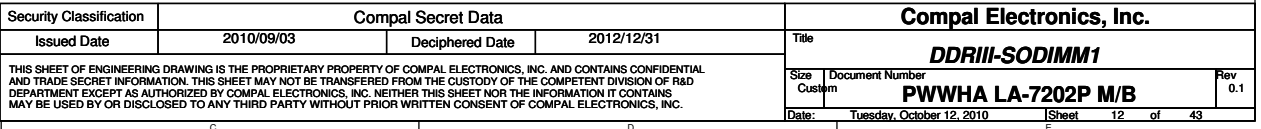
Bottom Socket Edge

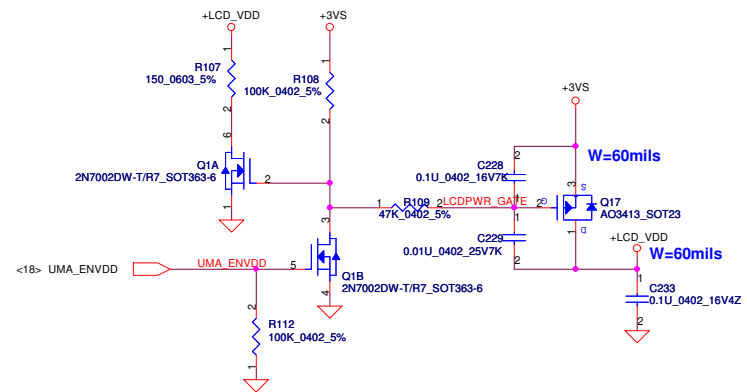
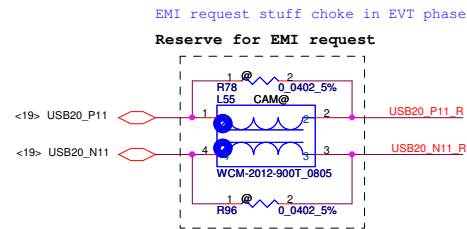
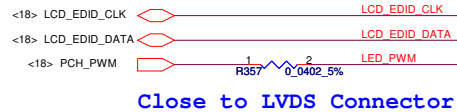


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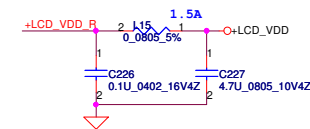
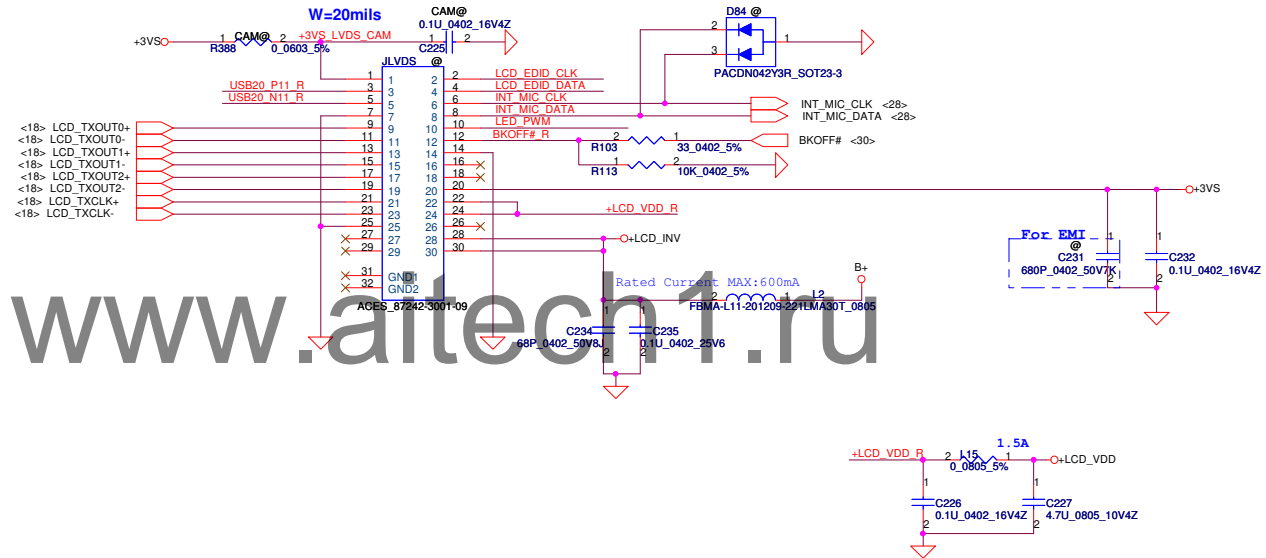




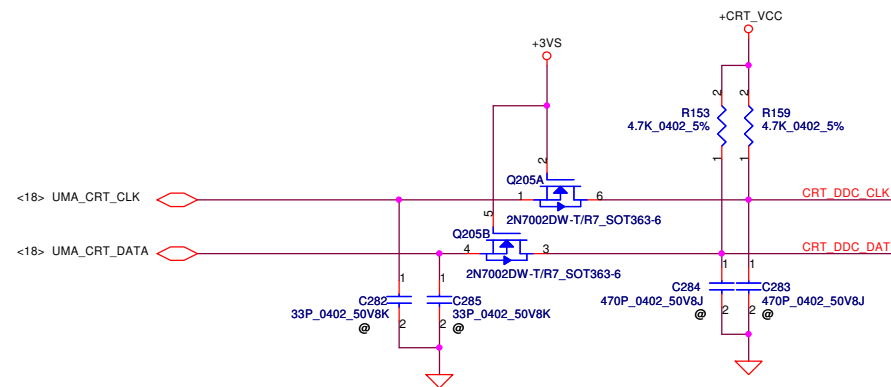
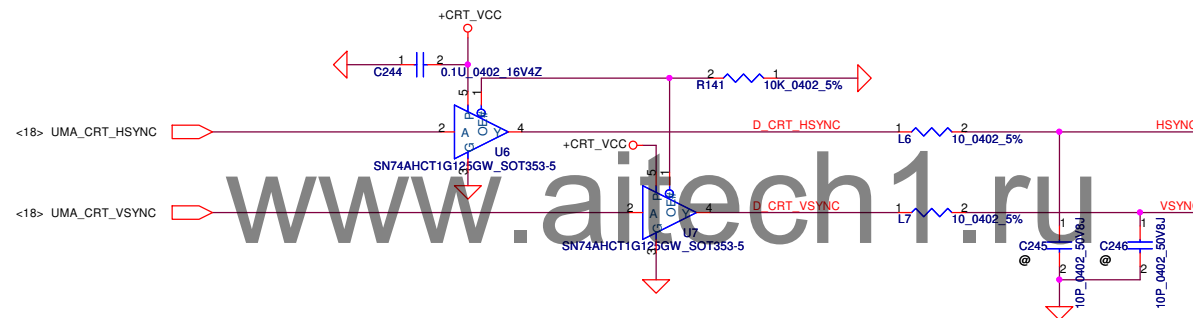
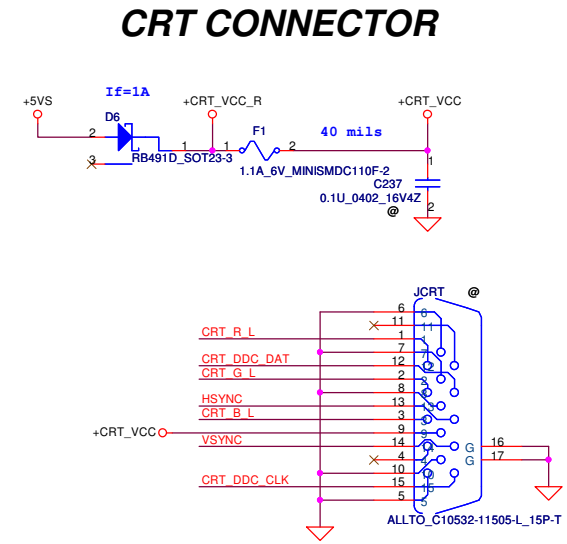
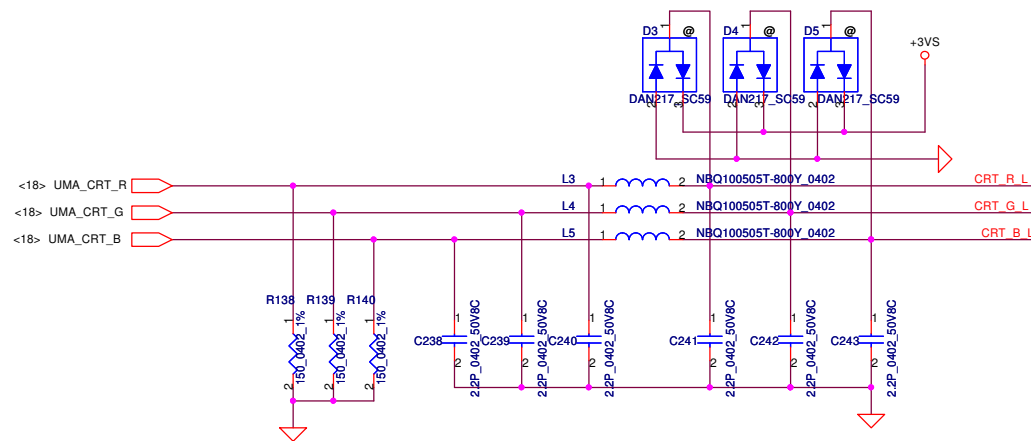




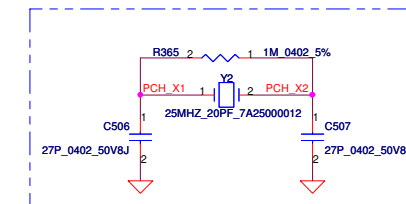
LCD/PANEL BD. Conn.



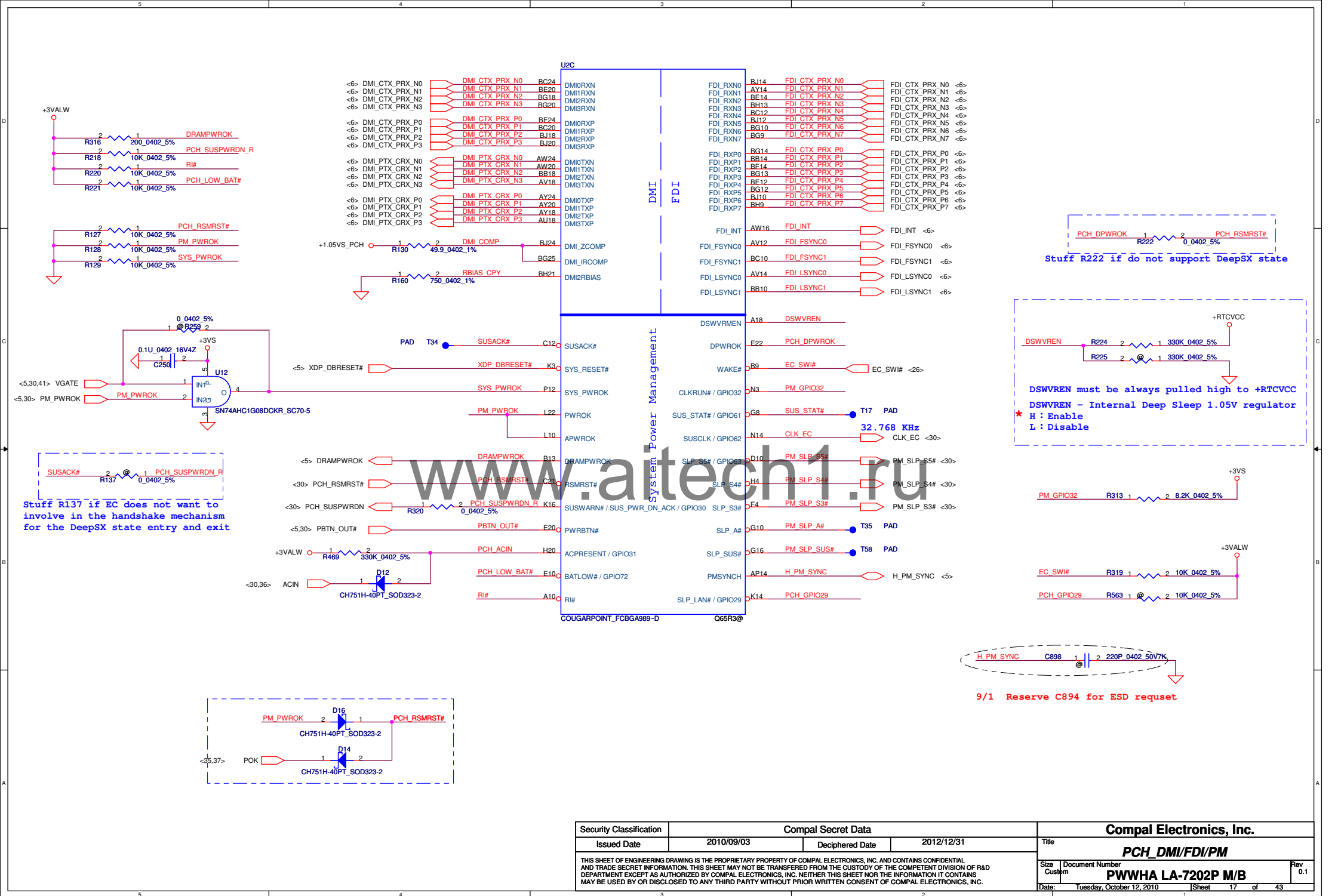
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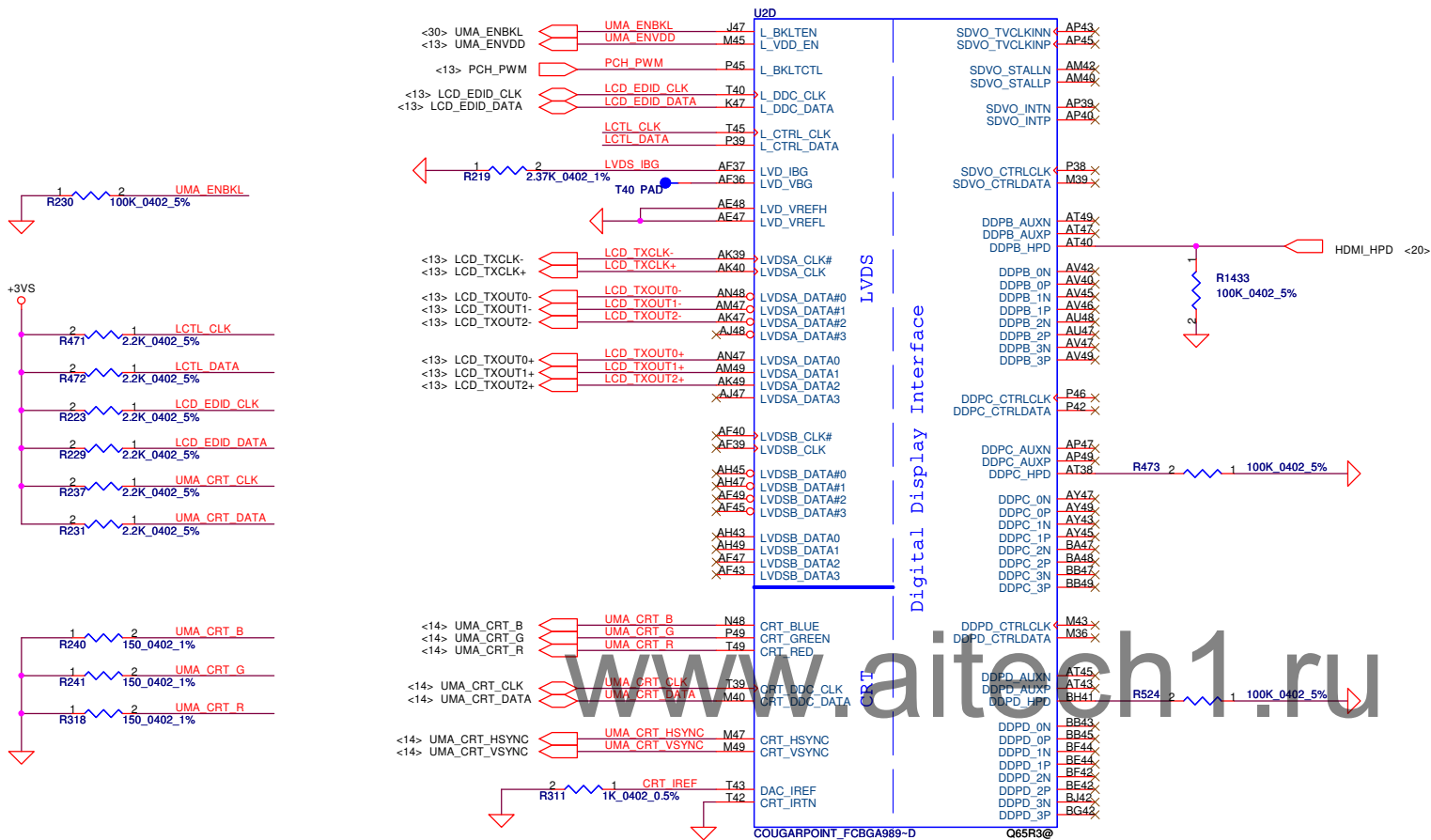
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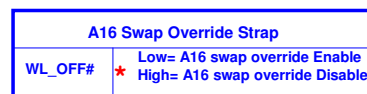
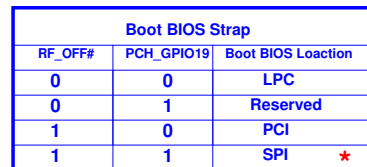
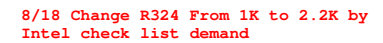
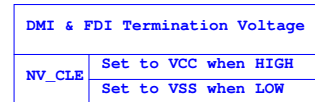
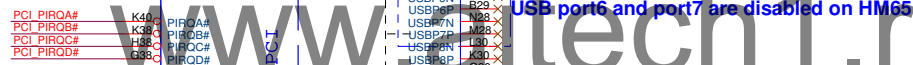
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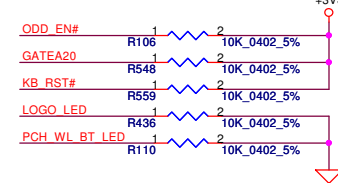
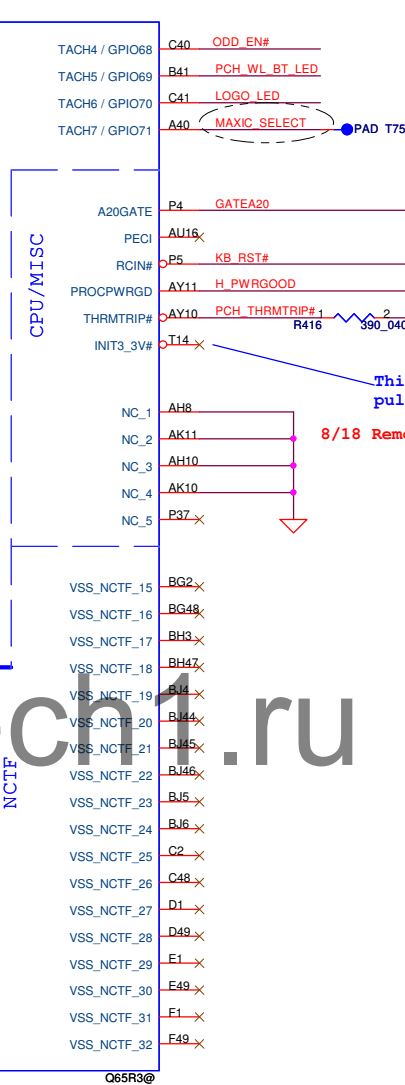
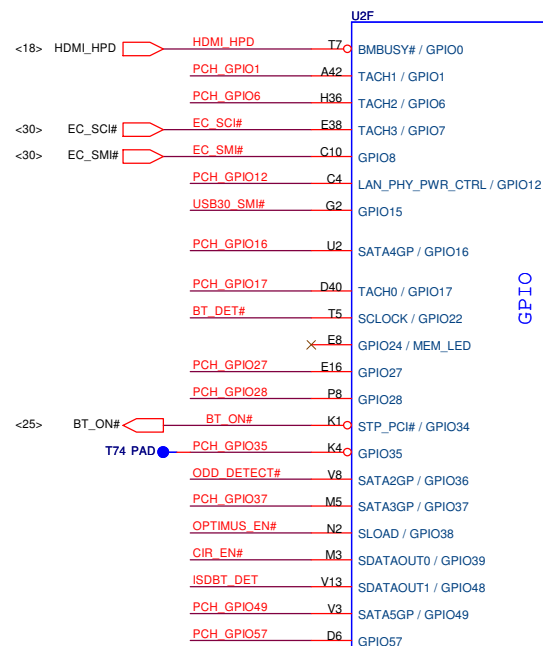
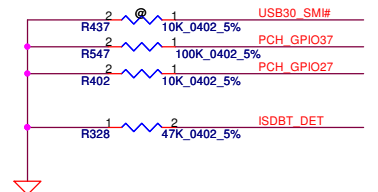
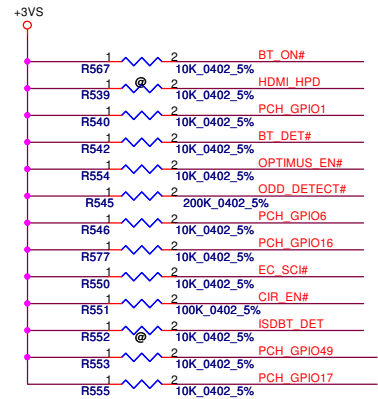
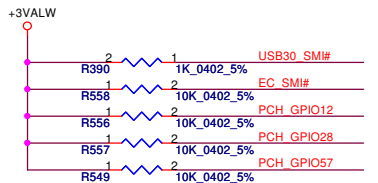
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Issued Date		Deciphered Date		Title	
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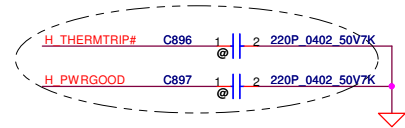
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Size	Custom	Document Number	PWWHA LA-7202P M/B	Rev	0.1
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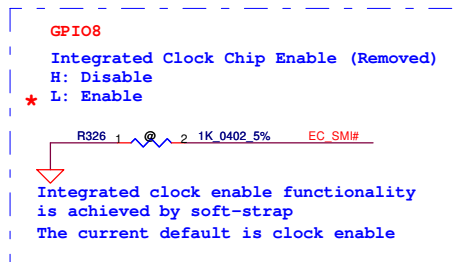
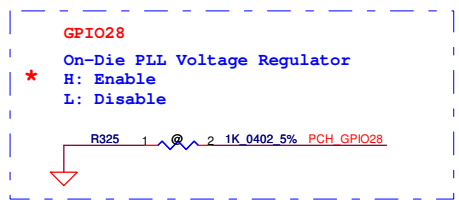
Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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				Size	Document Number
				Custom	PWWHA LA-7202P M/B
Date:		Tuesday, October 12, 2010	Sheet		19 of 43
					Rev 0.1



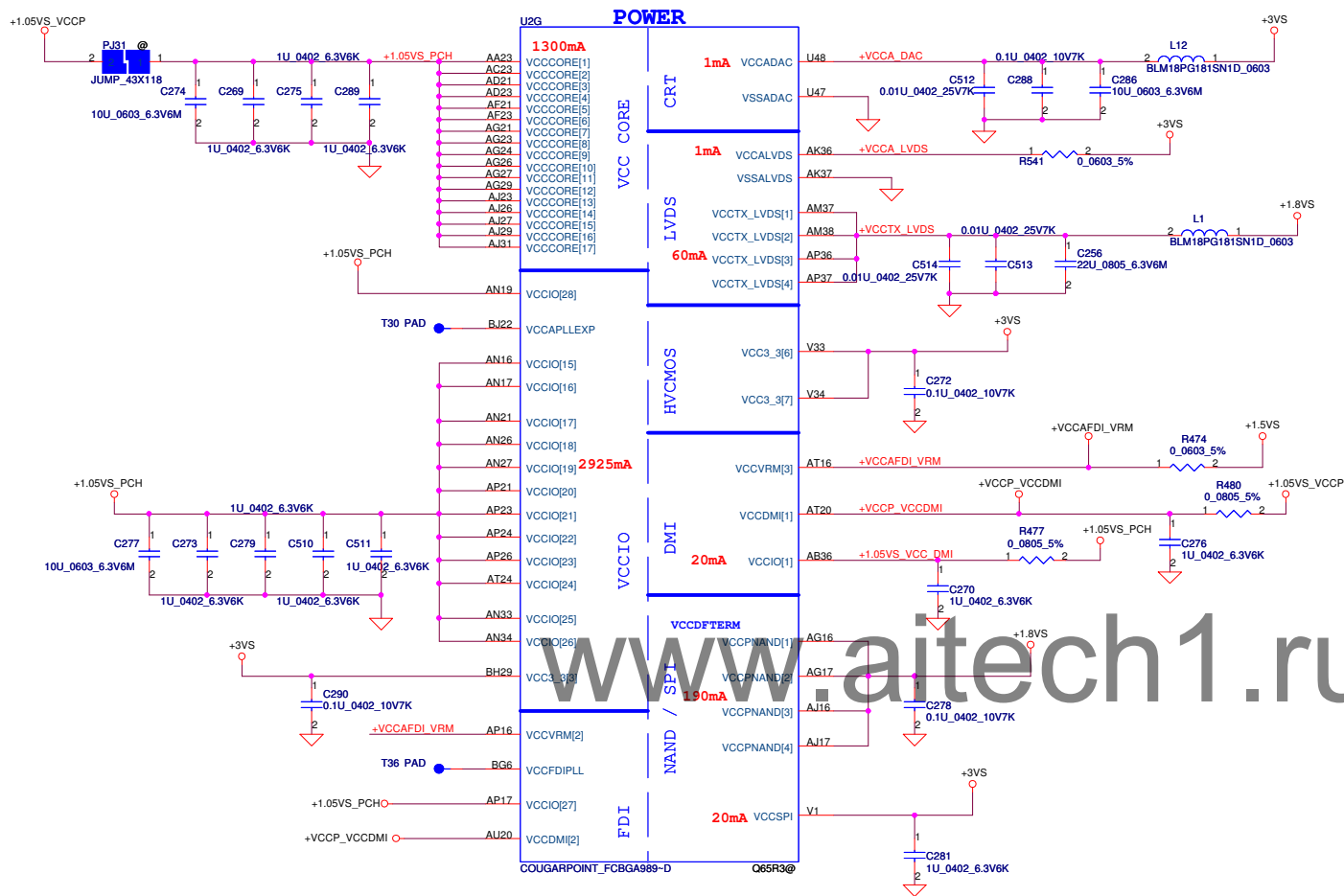
This signal has weak internal pull-up, can't be pulled low
8/18 Remove PCH Peci by HW Review demand



9/1 Reserve C896, C897 for ESD request

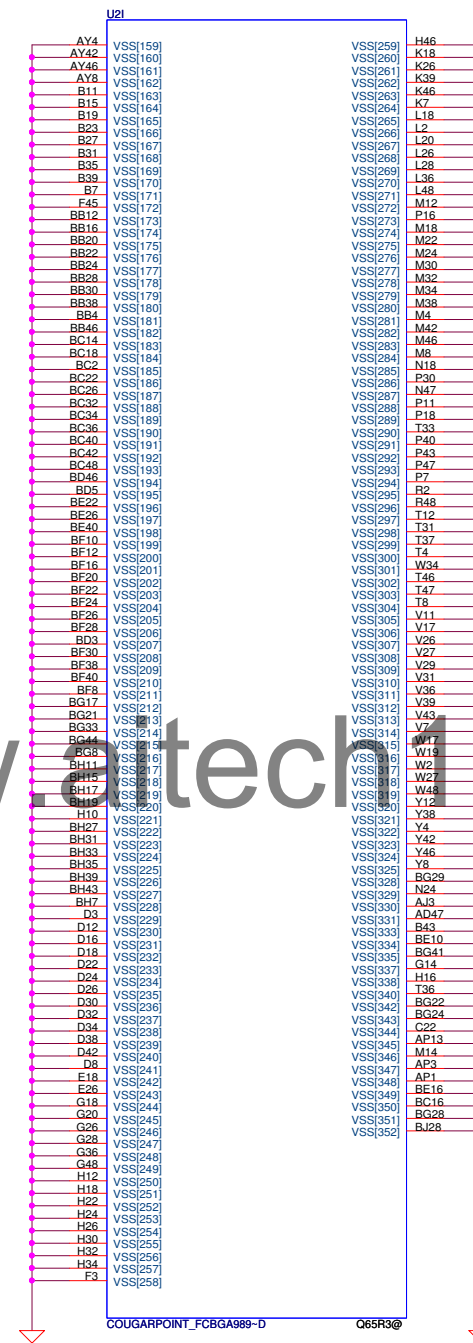
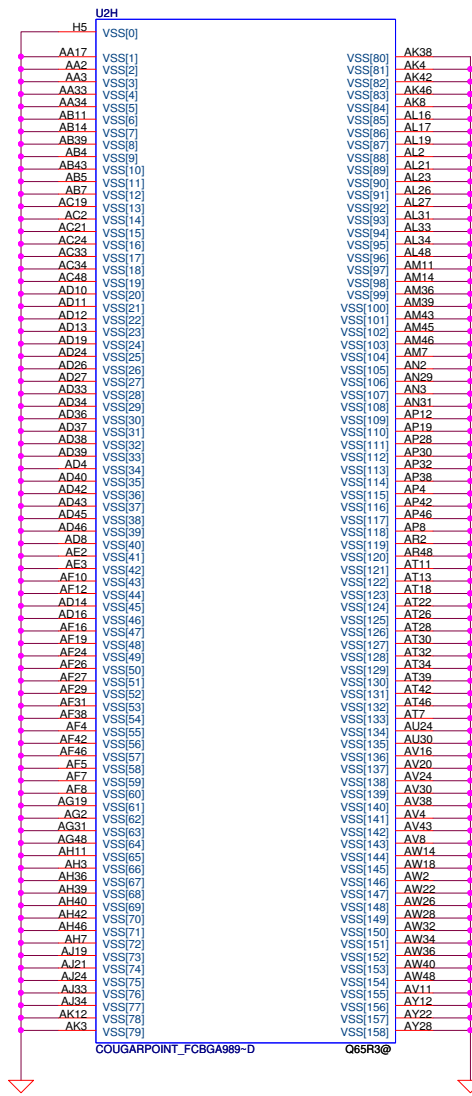


Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
				PCH_CPU/GPIO	
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				PWWHA LA-7202P M/B	
				Date:	Rev
				Tuesday, October 12, 2010	0.1
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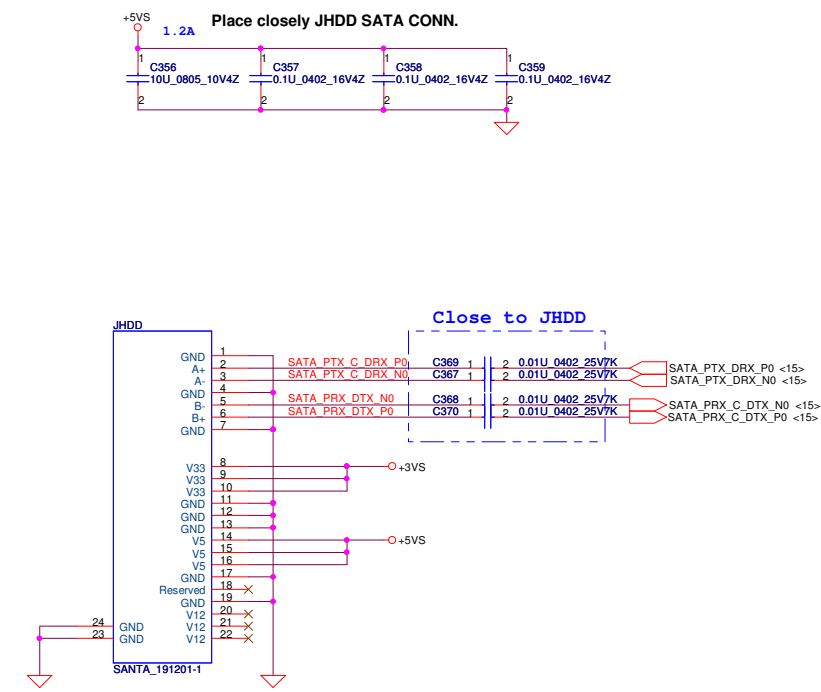
PCH Power Rail Table		
Voltage Rail	Voltage	S0 Iccmax Current (A)
V_PROC_IO	1.05	0.001
V5REF	5	0.001
V5REF_SUS	5	0.001
VCC3_3	3.3	0.266
VCCADAC	3.3	0.001
VCCADPILLA	1.05	0.08
VCCADPLL	1.05	0.08
VCCCORE	1.05	1.3
VCCDMI	1.05	0.042
VCCIO	1.05	2.925
VCCASW	1.05	1.01
VCCSPI	3.3	0.02
VCCDSW	3.3	0.002
VCCDFTerm	1.8	0.19
VCCRTC	3.3	6 uA
VCCSUS3_3	3.3	0.97
VCCSUSHDA	3.3 / 1.5	0.01
VCCVRM	1.5	0.16
VCCCLKDMI	1.05	0.02
VCCSSC	1.05	0.095
VCCDIFFCLKN	1.05	0.055
VCCALVDS	3.3	0.001
VCCTX_LVDS	1.8	0.06

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				Custom		PWWHA LA-7202P M/B					
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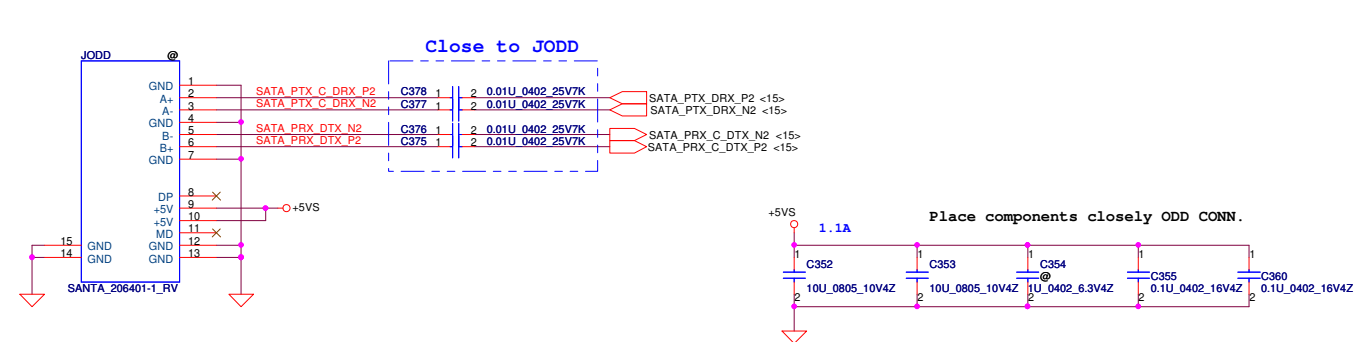


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Size	Document Number	PWWHA LA-7202P M/B		Rev	
Custom				0.1	
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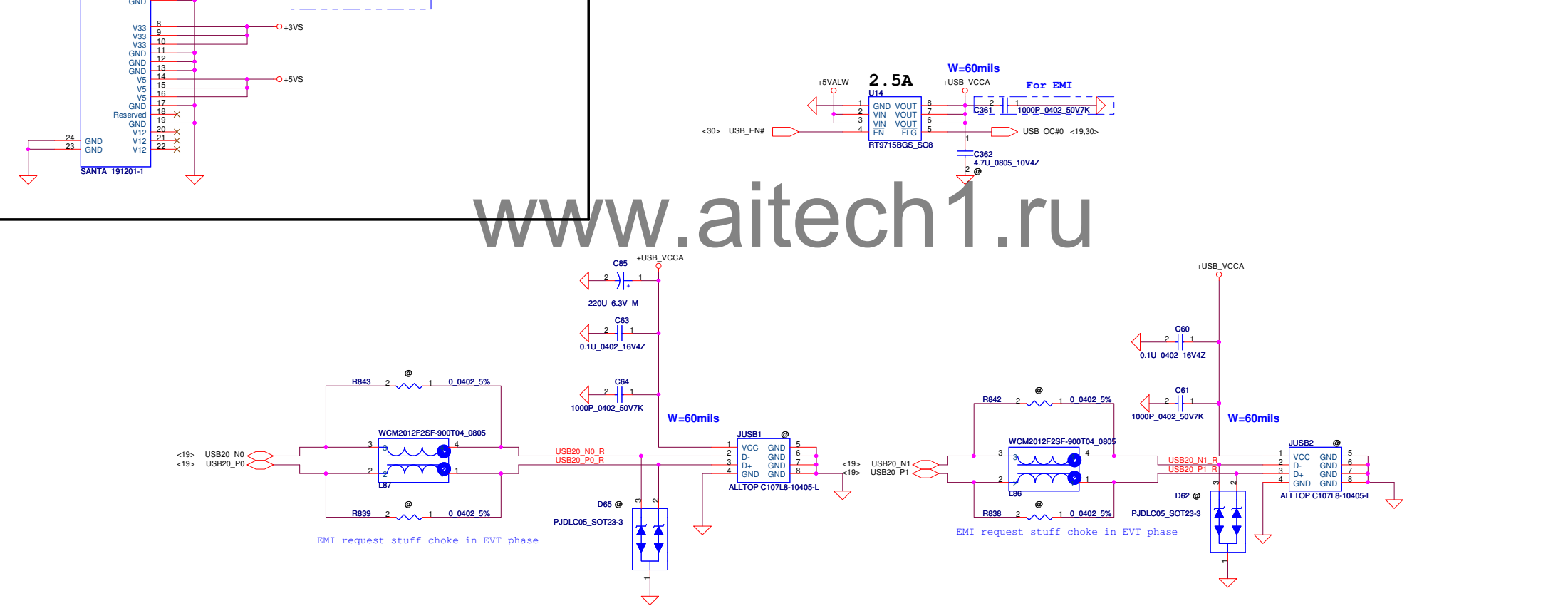
SATA HDD Conn



SATA ODD Conn

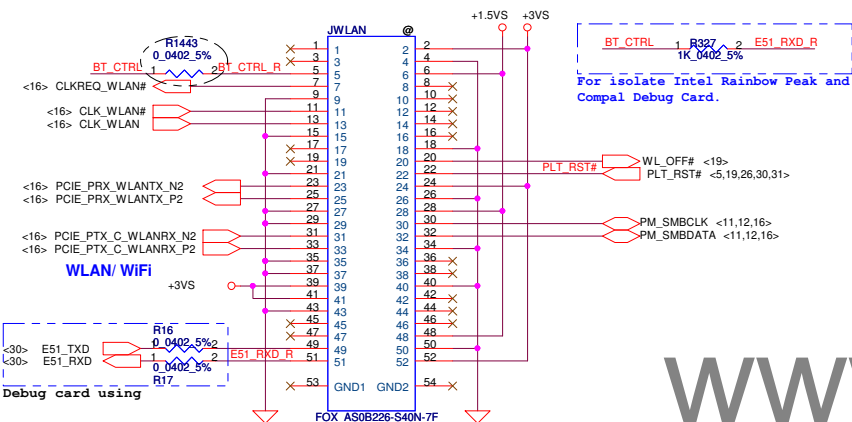
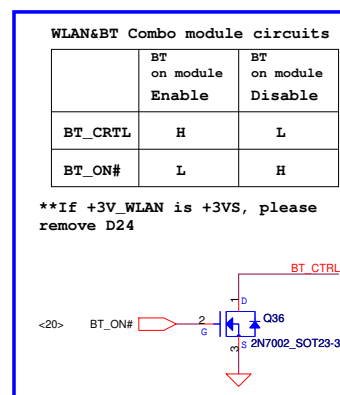
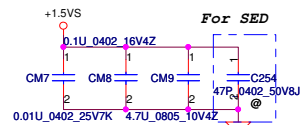
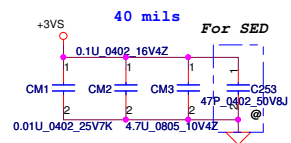


USB Conn



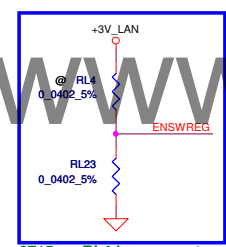
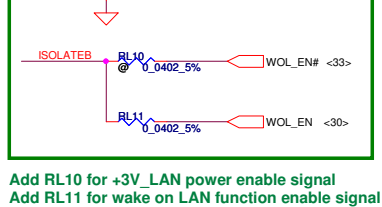
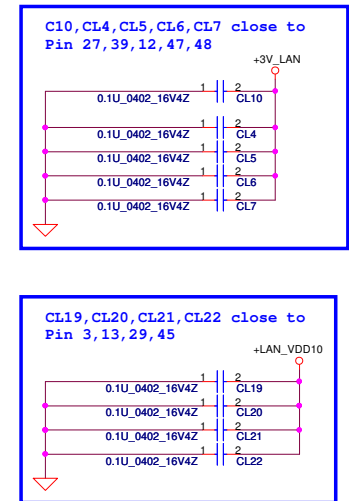
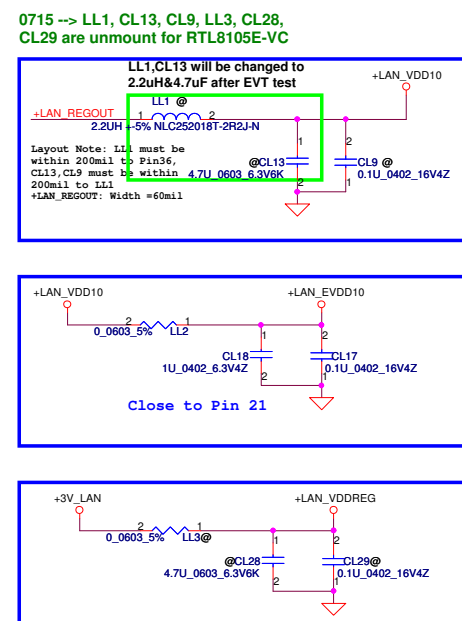
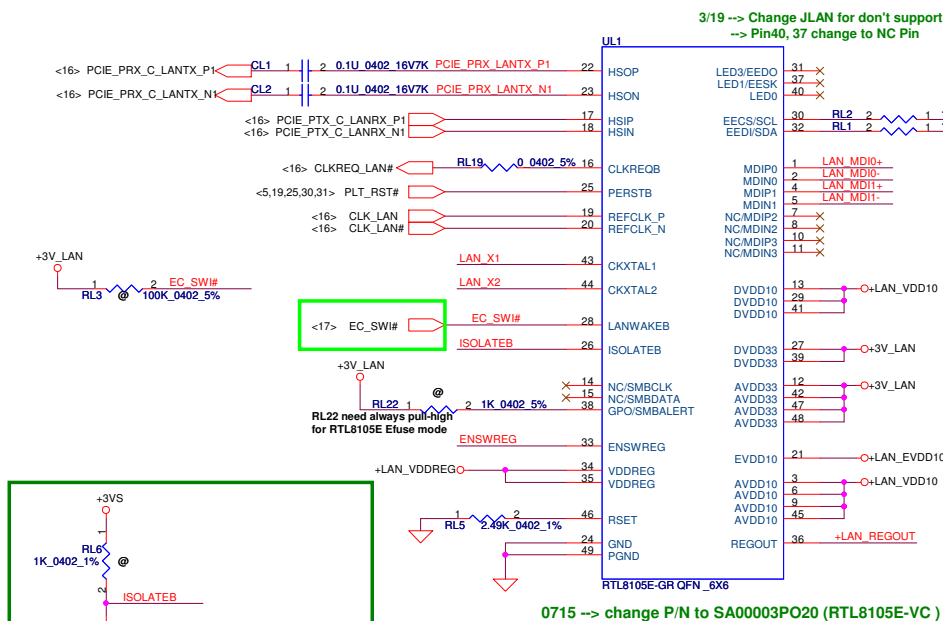
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Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title	
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Half PCIe Mini Card-WLAN



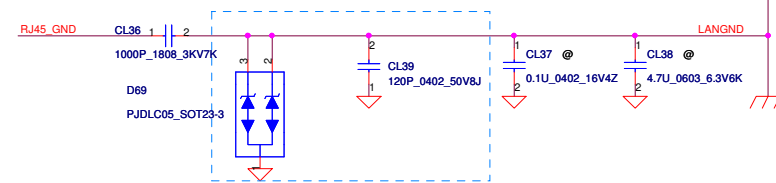
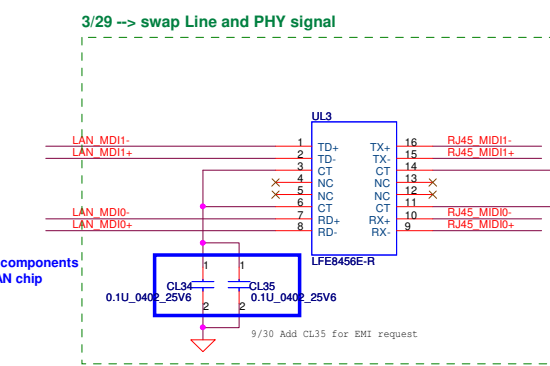
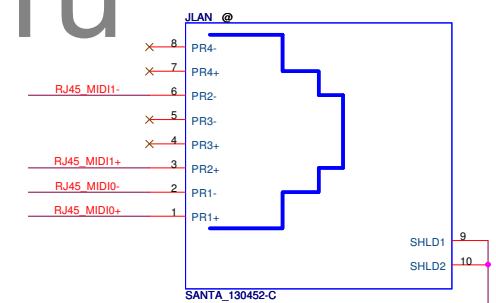
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				Size	Document Number	Rev
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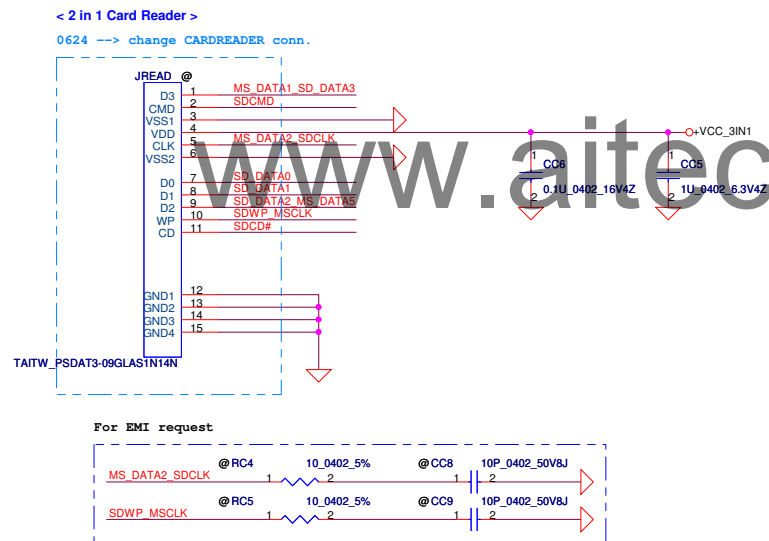
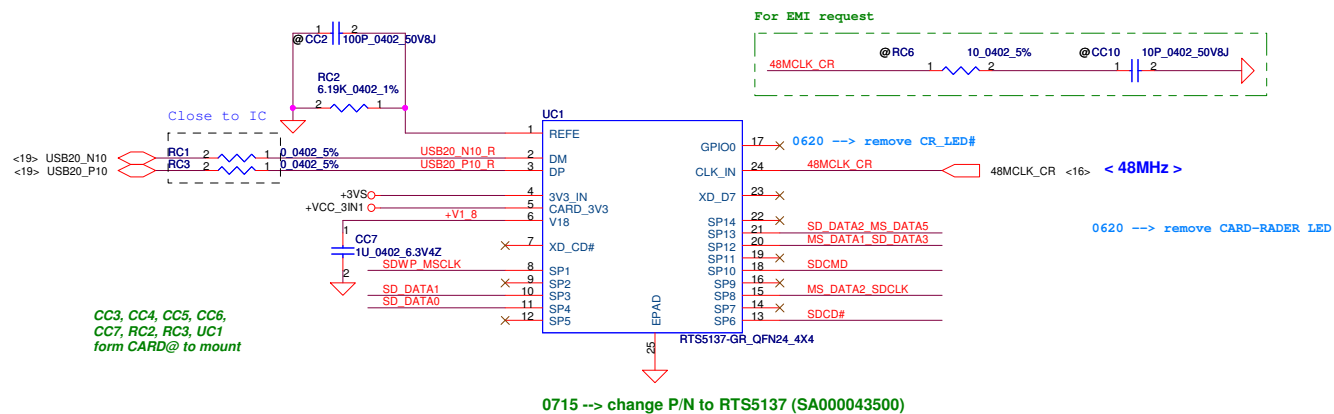


4/2-->remove RL8, RL9, CL11

LAN Conn.

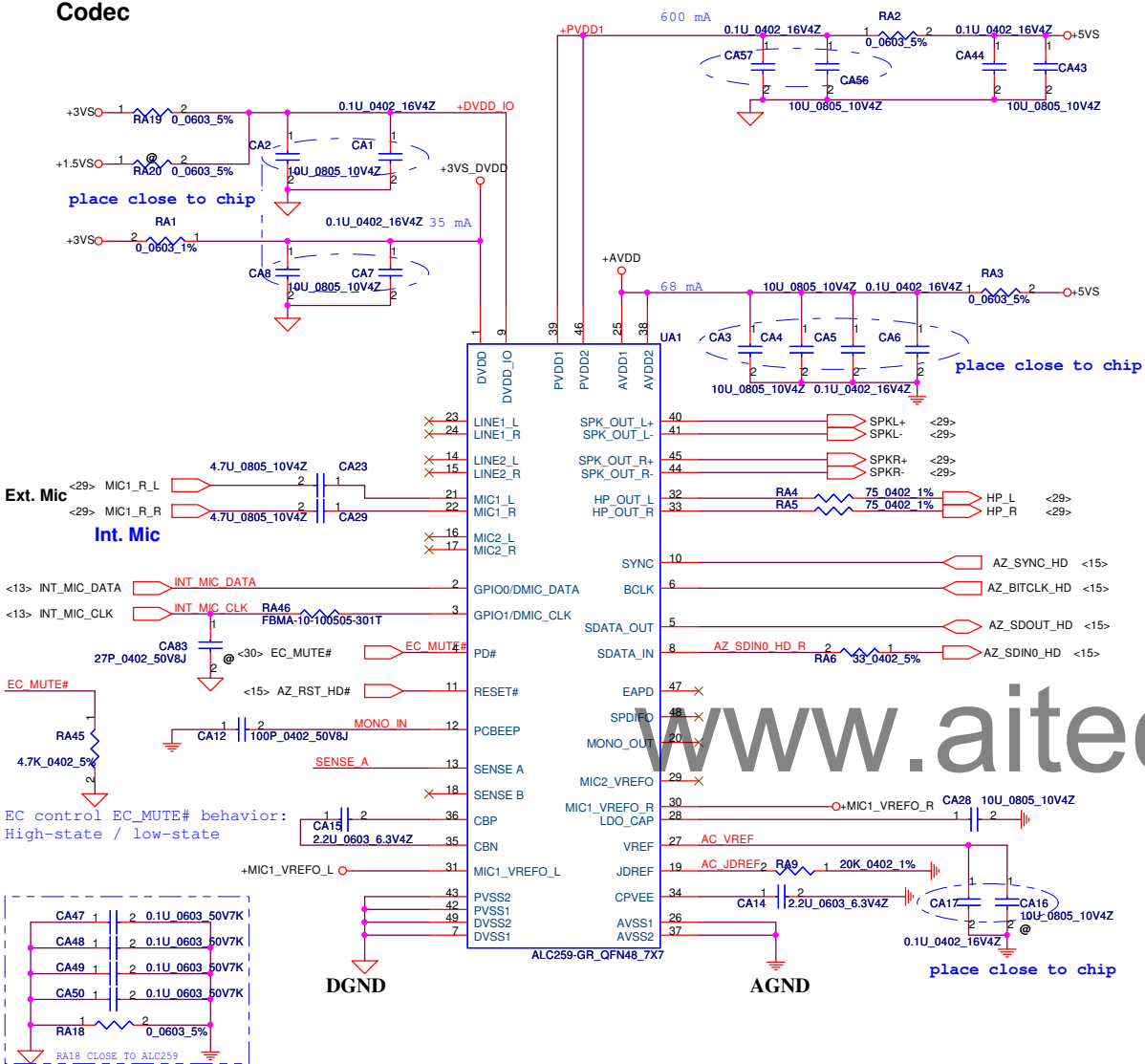


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Size	Document Number	PWWHA LA-7202P M/B		Rev 0.1	
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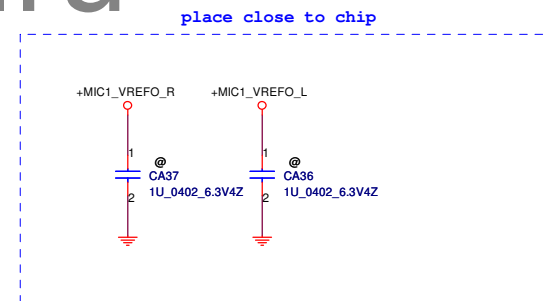
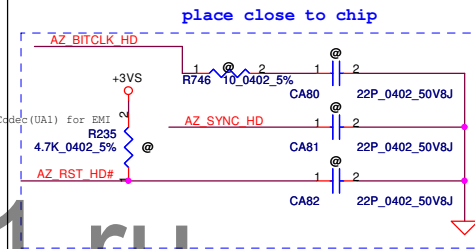
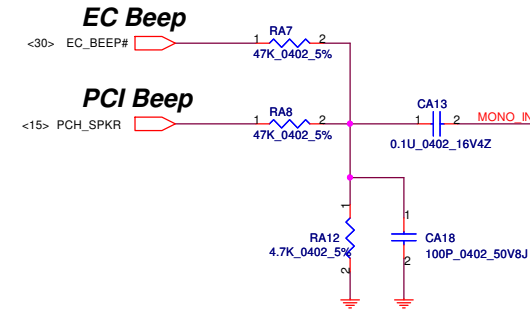


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Size	Custom	Document Number	PWWHA LA-7202P M/B	Rev	0.1
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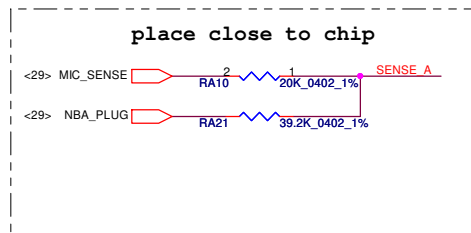
Codec



Beep sound



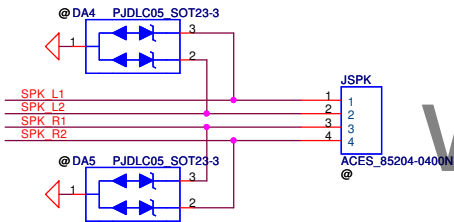
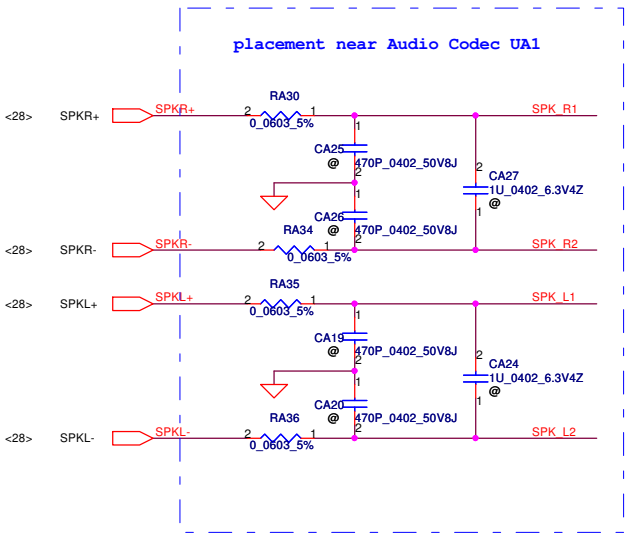
Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-I (PIN 32, 33)	Headphone out
	20K	PORT-B (PIN 21, 22)	Ext. MIC
	10K	PORT-C (PIN 23, 24)	
	5.1K	(PIN 48)	
SENSE B	39.2K	PORT-E (PIN 14, 15)	
	20K	PORT-F (PIN 16, 17)	Int. MIC
	10K	PORT-H (PIN 20)	



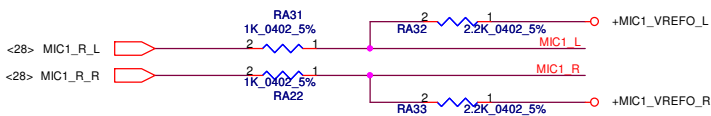
Security Classification				Compal Secret Data				Compal Electronics, Inc.			
Issued Date				2010/09/03				Deciphered Date			
2012/12/31				Title				HD CODEC ALC259			
Size				Document Number				PWWHA LA-7202P M/B			
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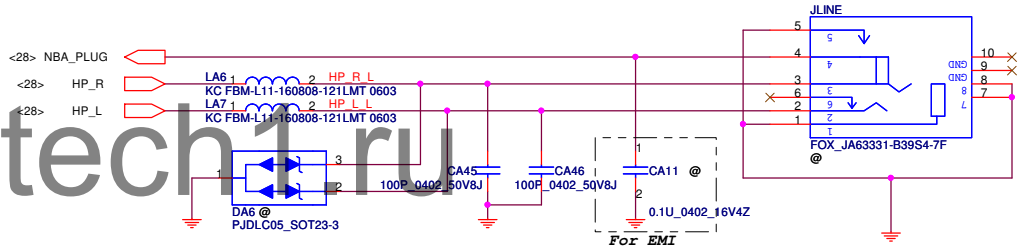
Speaker Connector



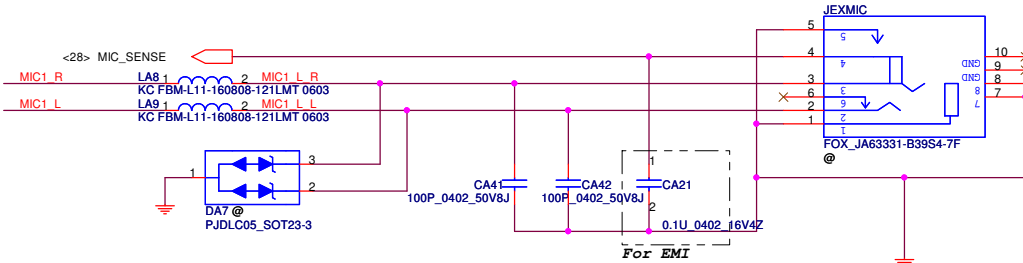
Ext. Mic



HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK



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3V1L

20mils

C451
0.1U_0402_16V4Z

U22
W25X10BVSNIG_S08

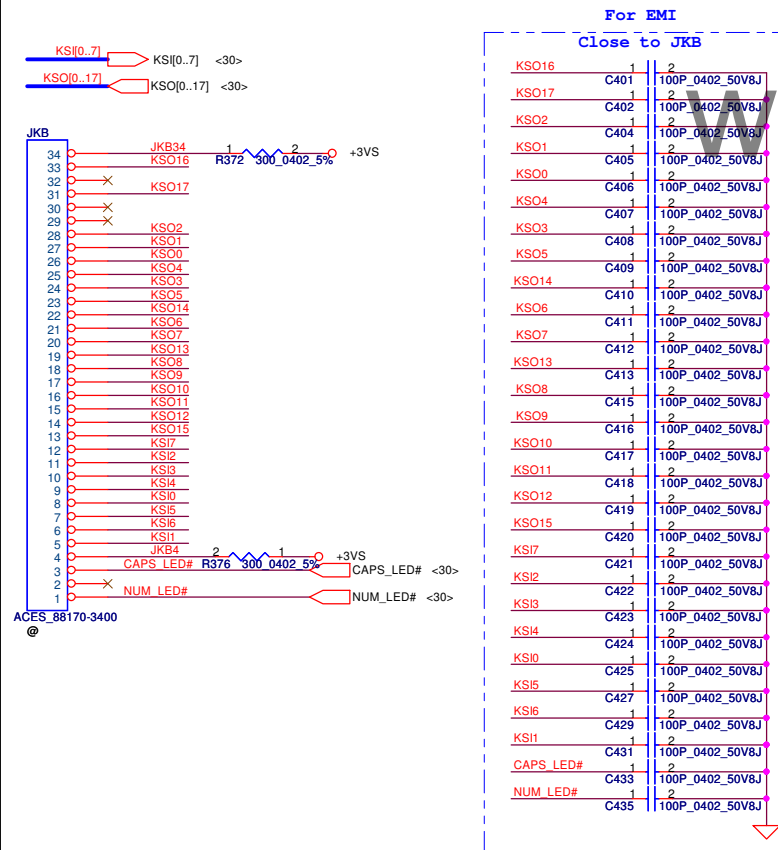
8 VCC
4 VSS
7 HOLD
1 CS
5 S
6 D
2 Q

<30> SPI_CS#
<30> SPI_CLK
<30> EC_SO_SPI_SI
EC_SI_SPI_SO <30>

R394
10_0402_5%
C454
10P_0402_50V6J

9/03 Change U22 change to SA00003FL10

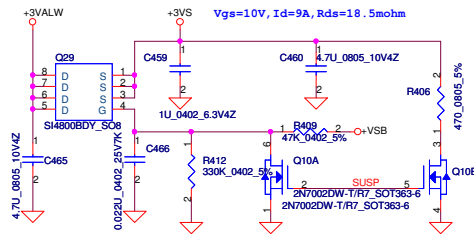
Noticed: KB Connector Pin Definition
Reversed with KB Membrane Pin Definition



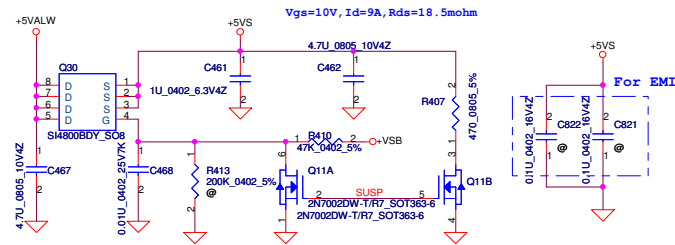
Security Classification	Compal Secret Data			Compal Electronics, Inc.		
Issued Date	2010/09/03	Deciphered Date	2012/12/31	Title SPI ROM/LID/Debug/KB		
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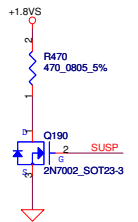
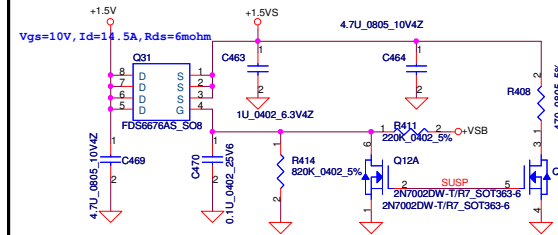
+3VALW TO +3VS



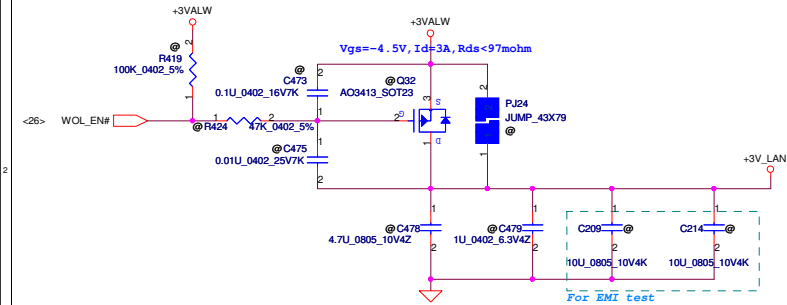
+5VALW TO +5VS



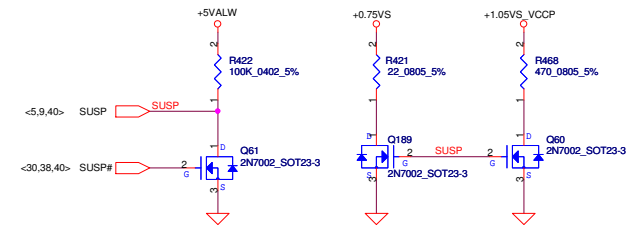
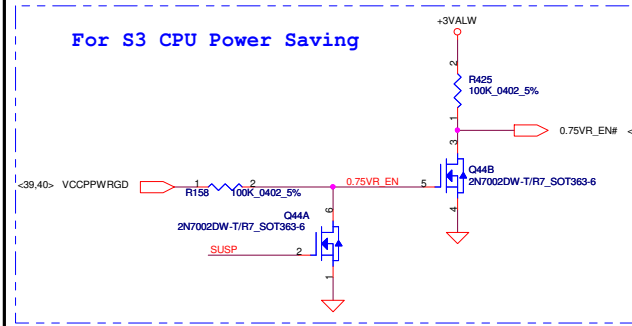
+1.5V to +1.5VS



+3VALW TO +3V_LAN



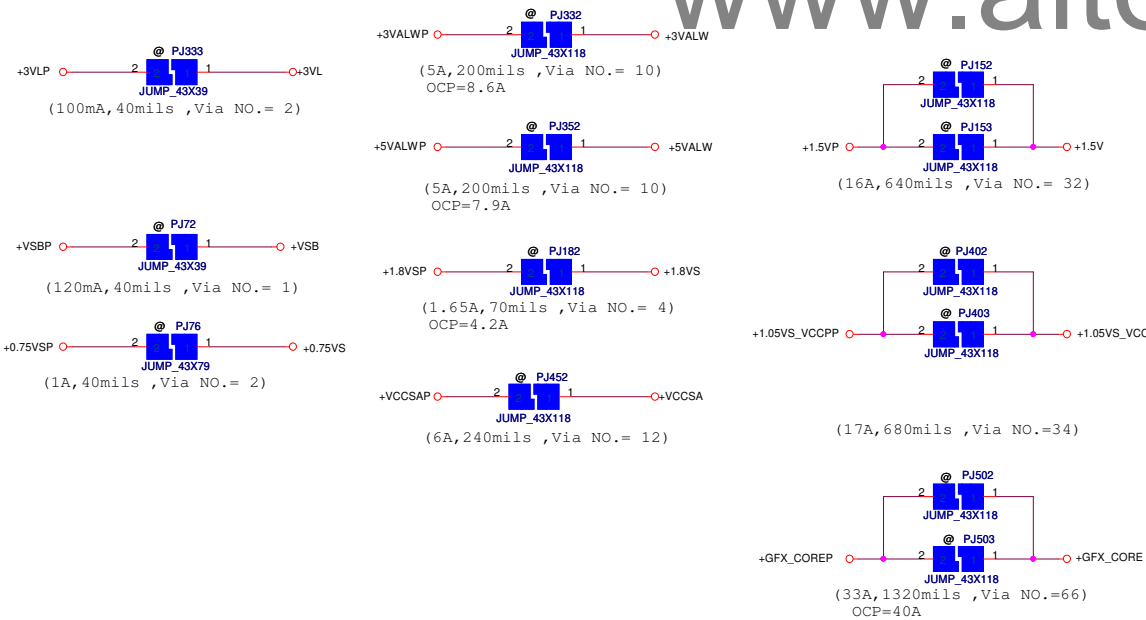
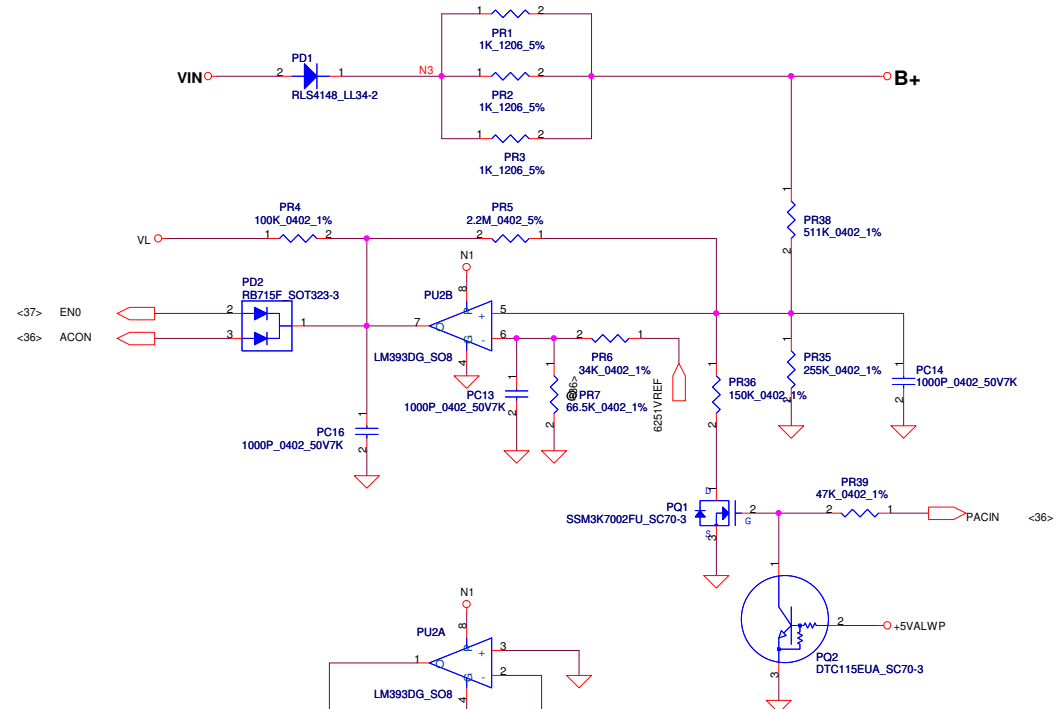
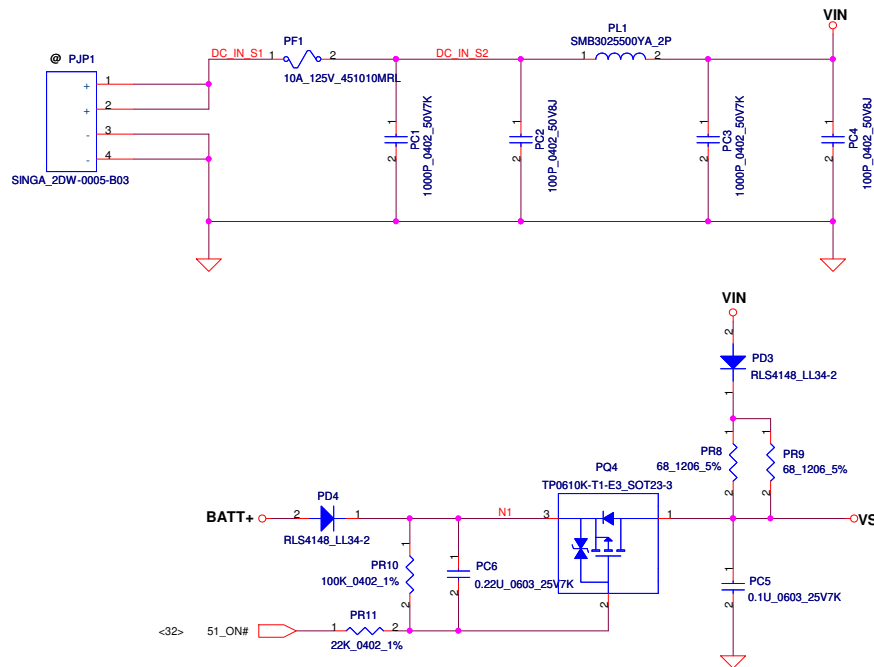
For S3 CPU Power Saving



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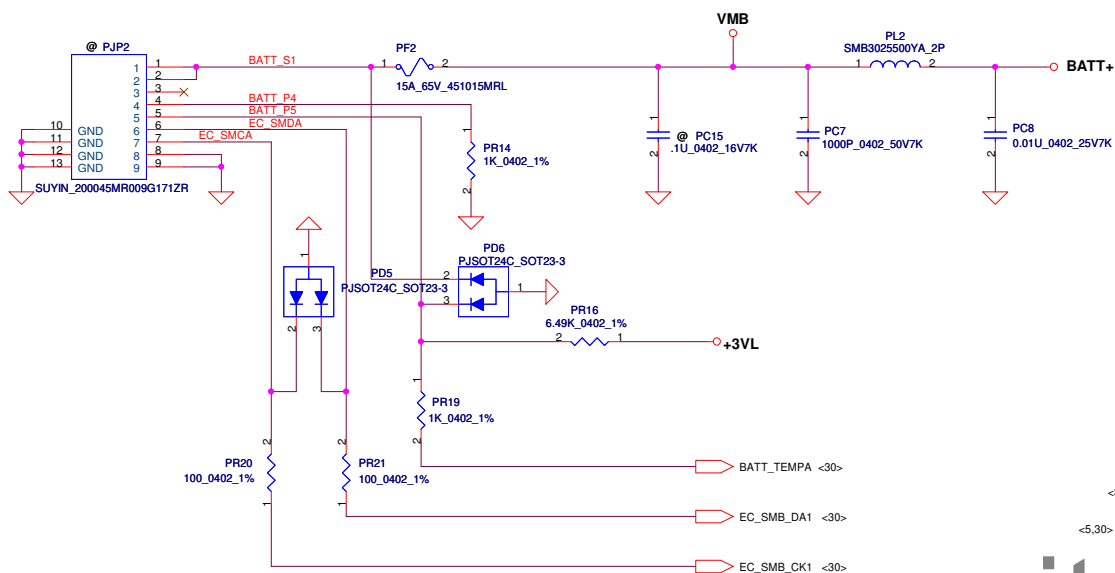
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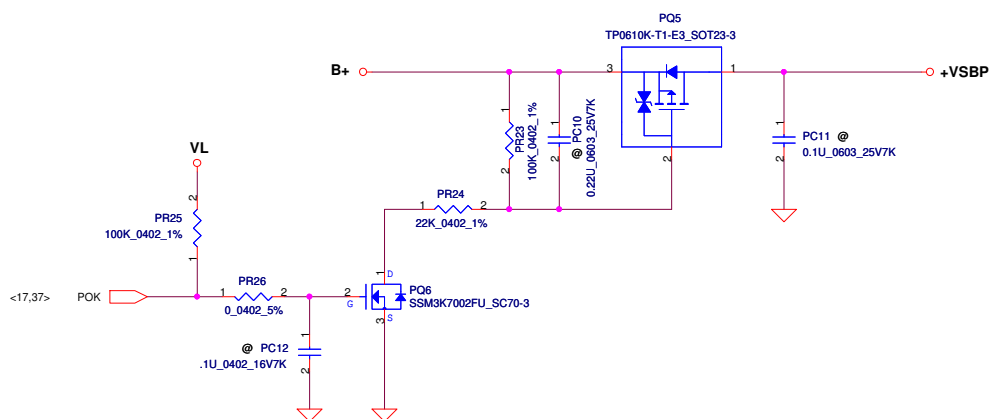
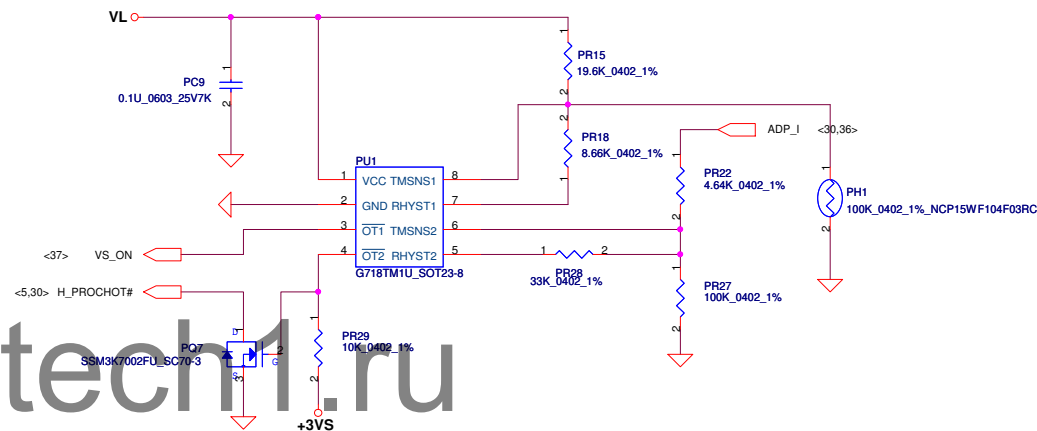


ACIN			
Precharge detector			
	Min.	typ.	Max.
H-->L	14.42V	14.74V	15.23V
L-->H	15.39V	15.88V	16.39V

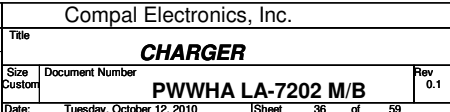
Security Classification		Compal Secret Data				Compal Electronics, Inc.					
Issued Date		2009/11/13		Deciphered Date		2009/04/28		Title			
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						Size		Document Number		Rev	
								PWWHA LA-7202 M/B		0.1	
						Date: Tuesday, October 12, 2010		Sheet 34 of 59			

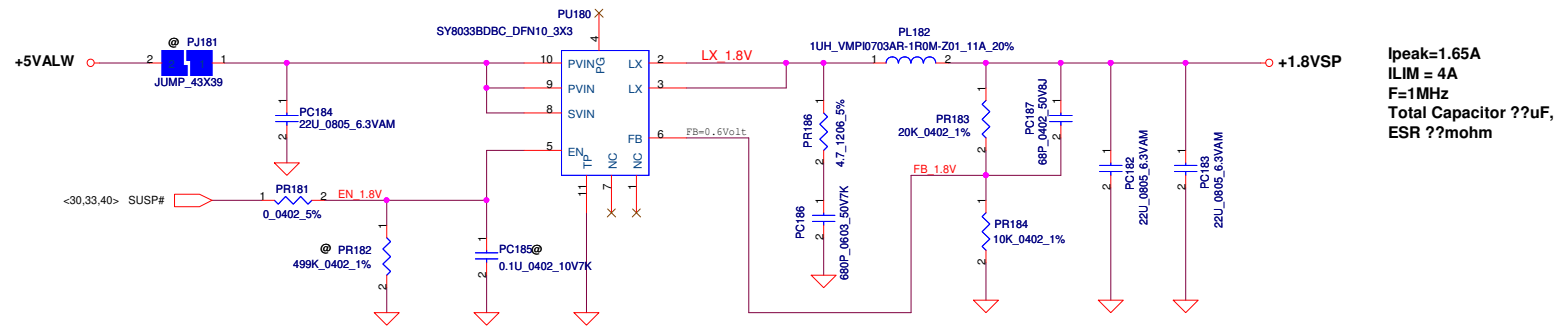
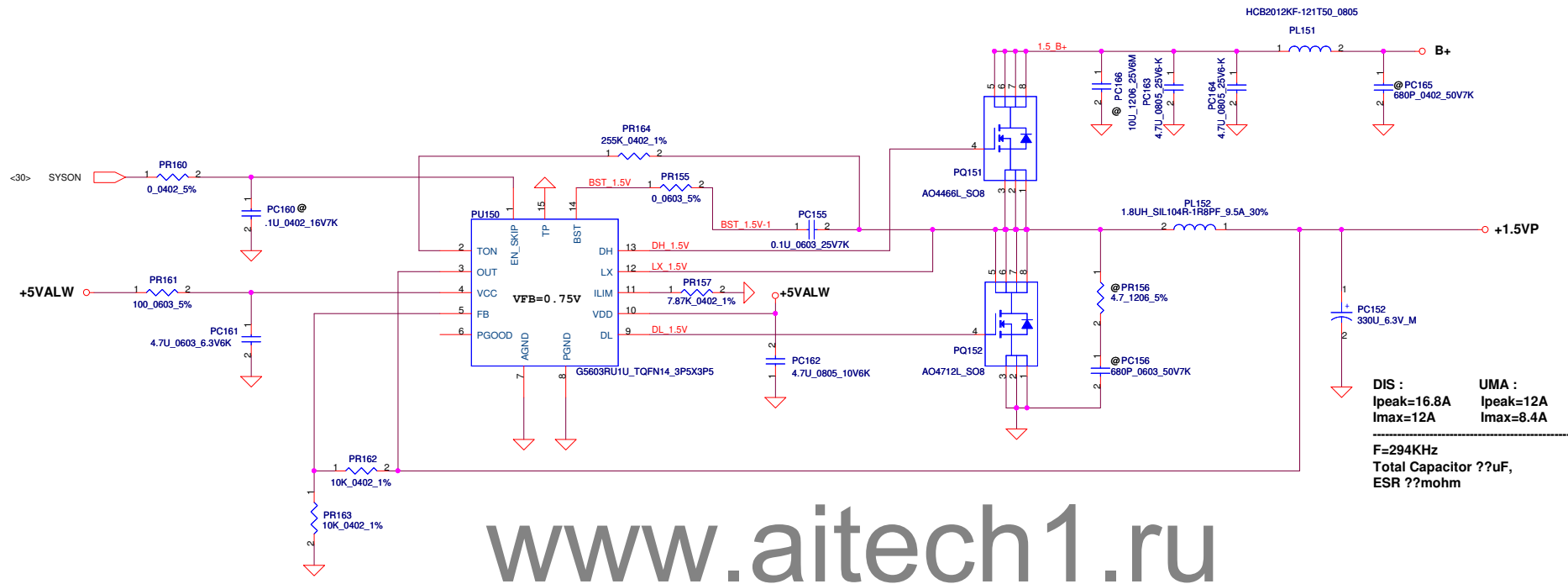


PH1 under CPU botten side :
CPU thermal protection at 95 degree C
Recovery at 56 degree C

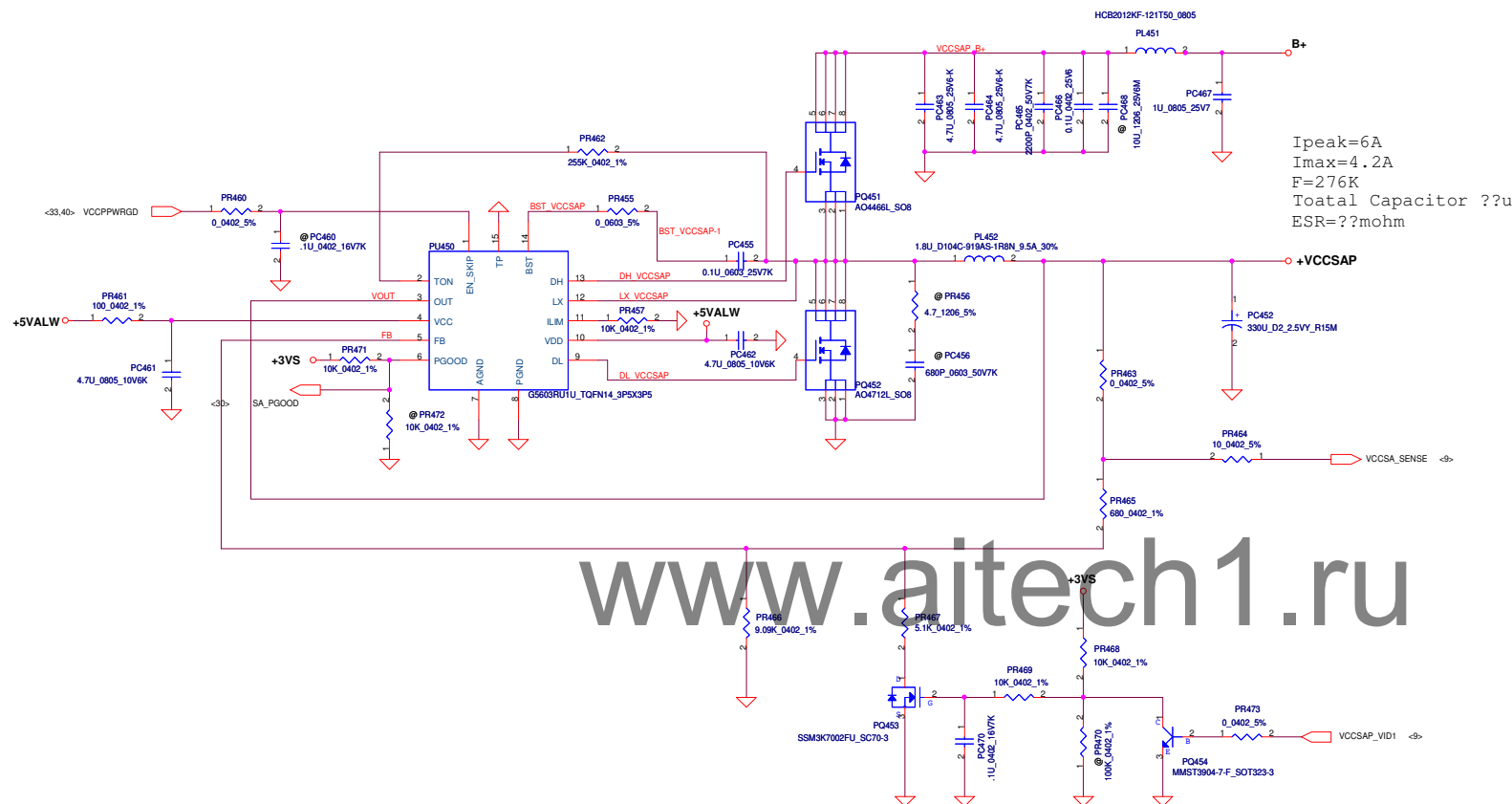


Adapter	Throttle Watt	Recovery Watt	Throttle Point	Recovery Point
65W_UMA	71.25W	62.4W	1.48V	1.308V
75W_DIS	85.5W	72W	1.78V	1.5V
75W_QCore	85.5W	72W	1.78V	1.5V





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Size	Custom	Document Number	PWWHA LA-7202 M/B	Rev	0.1
Date:	Tuesday, October 12, 2010	Sheet	38	of	59



Ipeak=6A
 Imax=4.2A
 F=276K
 Toatal Capacitor ??u
 ESR=??mohm

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VID1	+VCCSAP
1	0.8V
0	0.9V

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	2010/04/20	P36-P45	Release	

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Issued Date		2010/09/03	Deciphered Date	2012/12/31	
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		Power PIR			
		Size	Document Number		Rev
			NHQAA LA-6831P M/B		0.1
		Date:	Monday, October 11, 2010		Sheet 42 of 43

HW PIR (Product Improve Record)

NWQAA LA-7202P SCHEMATIC CHANGE LIST

REVISION CHANGE: 0.1

GERBER-OUT DATE: 2010/10/04

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1)	09/23	8	Remove C215, C219, C220	For layout region limitation
2)	09/23	15	Remove R572,R573,R574,R575,R569,U51,U52,C455,C456,U56,C249,R418,C483,R217,R227,R432,C482,R442,R443,D43,Q37,R226	Remove SPI flash circuit
3)	09/24	8	Remove C163, C153, C160,C152,C139,C138,C132	For layout region limitation
4)	09/24	10	Remove R241,R251,R261,R271,R191,R201,R211,R231	For Huron River common design
5)	09/24	21	Remove R483,C280,L22,C509	For layout region limitation
6)	09/24	21	Change L1 size from 1608 to 0603	For layout region limitation
7)	09/24	22	Remove L20,C302,R498,L17,C296	For layout region limitation
8)	09/24	22	Change R509,R517,R520 size from 0603 to 0402	For layout region limitation
9)	09/24	24	Remove SW5,R561,R562	No support zero power ODD function
10)	09/24	27	Remove RC3,CC4,CC3	For Card Reader IC common design
11)	09/24	28	Remove RA11,CA63,CA62,CA58	For Audio CODEC IC common design
12)	09/24	30	Remove R380,R382	ENE has fixed entry test mode issue
13)	09/24	33	Remove R457,Q53,Q51,Q45,PJ28,R441,R440,C471,C217,C679,C680	No support zero power ODD function
14)	09/27	12	Remove C189	For layout region limitation
15)	09/27	25	Remove PJ26,PJ27	No support WiMAX function
16)	09/27	30	Remove R389,C449,C450,Y4,R565	Due to use internal clock generator, removed for layout region limitation
17)	09/28	17	Remove R216	Remove for layout region limitation
18)	09/28	25	Remove D24	No support WiMAX function
19)	09/28	13	Remove R358	Backlight control by PCH
20)	09/29	32	Remove SW2	For more placement space
21)	09/30	26	Add CL35	For EMI request
22)	10/04	30	Add R738,C449	For EMI request
23)	10/04	27	Add R739,R740	For USB EA test used
24)	10/05	17	Remove R566	For using internal SUSCLK to EC
25)	10/05	15	Add R1444	Intel recommand use 1M ohm on A2_SYNC to PD
26)	10/05	28	Remove JA1	Use the same power rail on CODEC
27)	10/05	19	Change from USB_OC#3 to SLP_CHG_M3	For HW common design
28)	10/05	19	Change from USB_OC#4 to SLP_CHG_M4	For HW common design
29)	10/05	19	Change from SLP_CHG_M3 to USB_OC#5	For HW common design
30)	10/05	19	Change from SLP_CHG_M4 to USB_OC#6	For HW common design
31)	10/06	16	Remove R417,C474	For EMI request
32)	10/06	5	Change FAN control from DC mode to PWM mode	Change FAN control circuit
33)	10/07	33	Change package of Q6A from SOT363 to SOT23	To get more layout space
34)	10/08	16	Add R417,C474	For EMI request
35)	10/11	9	Change R122,R252 from 100 ohm to 1K ohm	For Intel Design Guide
36)	10/11	27	Change location from R739,R740 to RC1,RC3	For naming rule
37)	10/11	28	remove CA61	For Audio CODEC common design
38)	10/11	30	Add R1445	To avoide PLT_RST# floating
39)	10/11	30	Add R1446,C899	Recommand from ENE
40)	10/11	16	Change R228 from 10k ohm to 1k ohm	Follow Intel Check List
41)	10/11	26	RL22 no stuff	Follow Realtek Design Guide
42)	10/12	31	Modify Lid Switch power rail	For avoide EC issue